



A program logic for system verification

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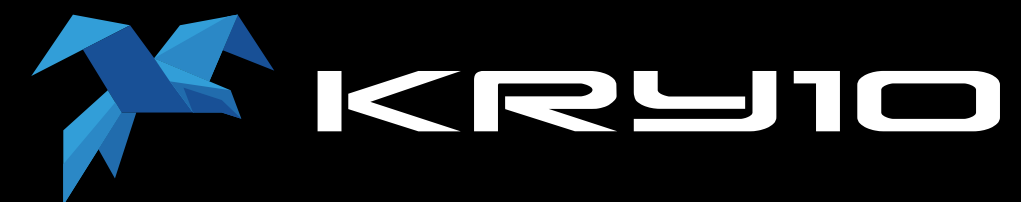
Kry10

seL4 Summit – 3 September 2025 – Prague

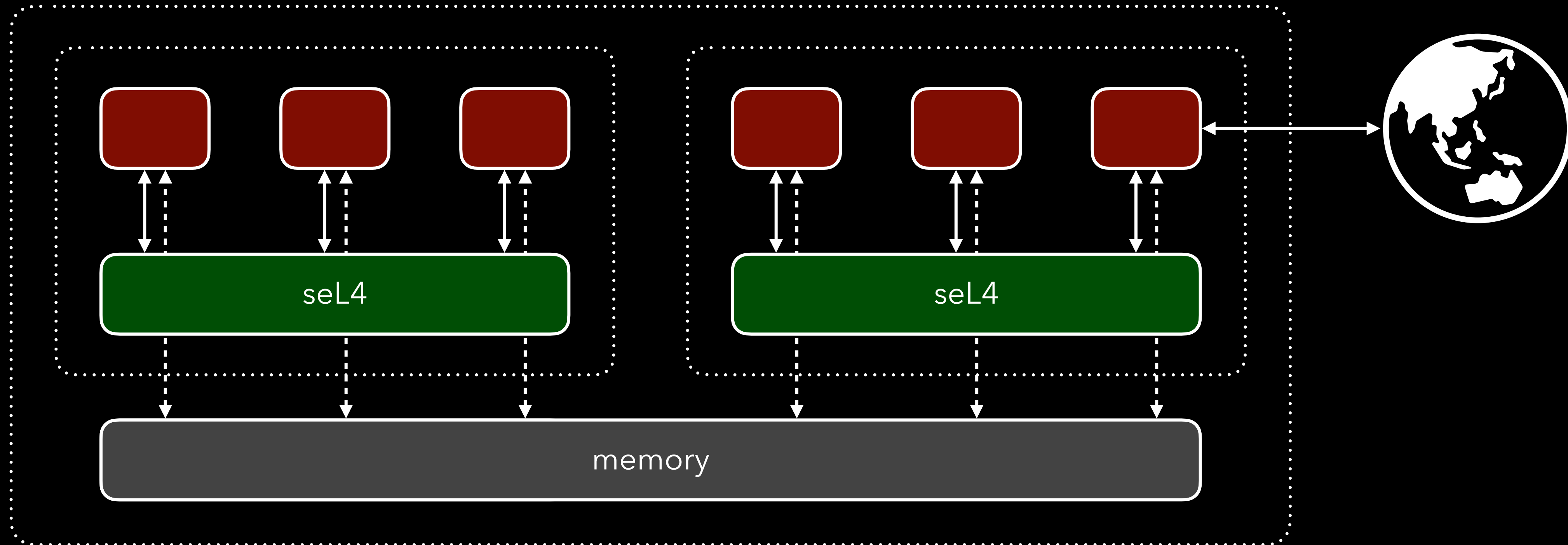


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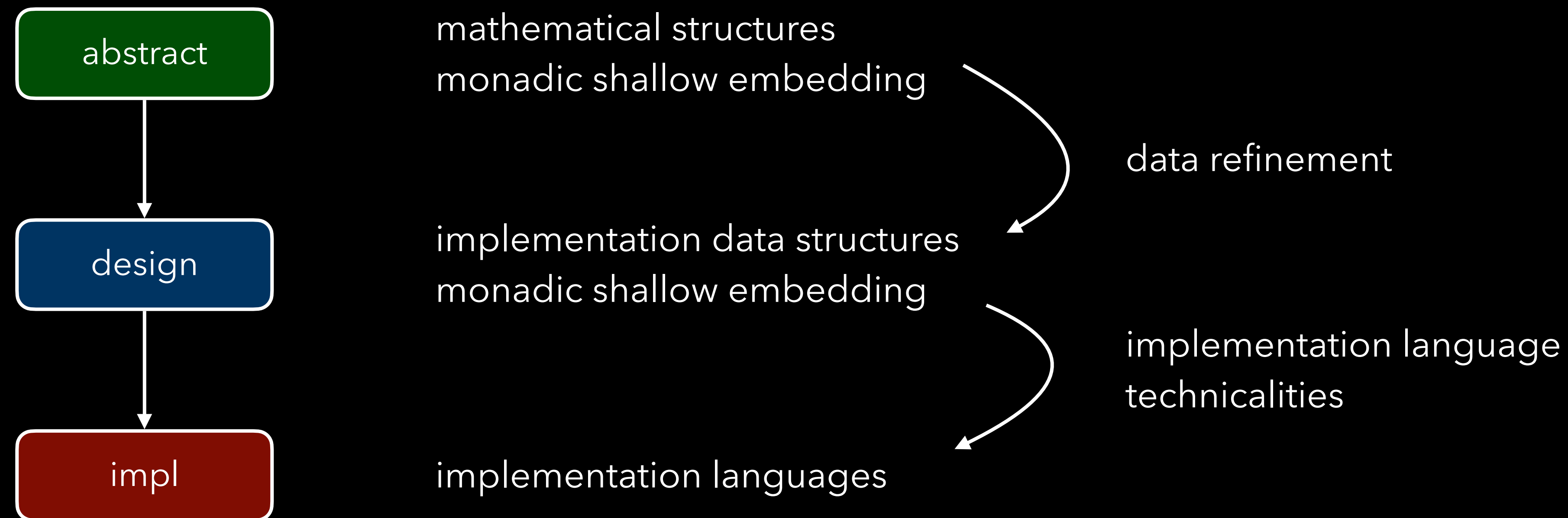
What is a system?



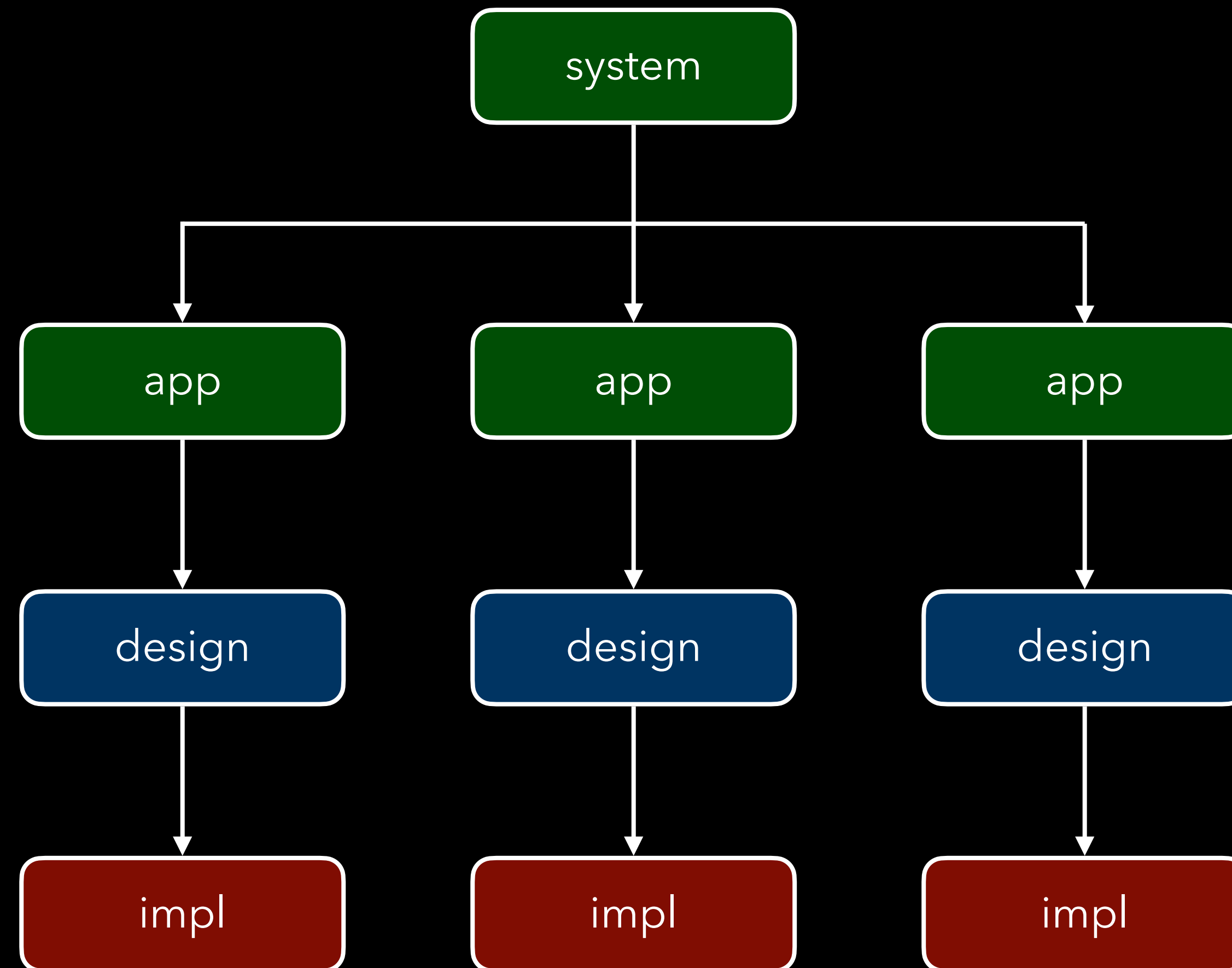
- Composition
- Internal & external interaction

What is system verification?

(seL4 verification recap)



What is system verification?



refinement from
sequential system spec to
concurrent app specs

What is system verification?

1. Specification language
 - system and application specifications
2. Semantics
 - define system states
 - define how they execute
3. Program logic
 - reason about applications and systems
 - prove refinement

Interaction trees
(Xia et al. 2020)



Iris separation logic
(Jung et al. 2015)

Specifications as interaction trees



```
adder (ep_slot reply_slot : slot) (sum : word) :=  
  x ← ep_recv ep_slot reply_slot ;  
  ep_reply reply_slot sum ;  
  adder ep_slot reply_slot (sum + x)
```

Specifications as interaction trees



```

adder (ep_slot reply_slot : slot) (sum : word) :=
  x ← ep_recv ep_slot reply_slot ;
  ep_reply reply_slot sum ;
  adder ep_slot reply_slot (sum + x)
  
```

```

Variant invocation : Type → Type :=
  | EP_Recv (ep_slot reply_slot : slot)
    : invocation word
  | ...
  
```

```

ep_recv (ep_slot reply_slot : slot)
  : itree invocation word :=
  trigger (EP_Recv ep_slot reply_slot)
  
```


Specifications as interaction trees



```

adder (ep_slot reply_slot : slot) (sum : word) :=
  x ← ep_recv ep_slot reply_slot ;
  ep_reply reply_slot sum ;
  adder ep_slot reply_slot (sum + x)
  
```

```

client (ep_slot mmio_slot : slot) :=
  x ← read mmio_slot ;
  r ← ep_call ep_slot x ;
  write mmio_slot r ;
  client ep_slot mmio_slot
  
```

Specifications as interaction trees



```

adder (ep_slot reply_slot : slot) (sum : word) :=
  x ← ep_recv ep_slot reply_slot ;
  ep_reply reply_slot sum ;
  adder ep_slot reply_slot (sum + x)

```

```

client (ep_slot mmio_slot : slot) :=
  x ← read mmio_slot ;
  r ← ep_call ep_slot x ;
  write mmio_slot r ;
  client ep_slot mmio_slot

```

```

spec (mmio_slot : slot) (sum : word) :=
  x ← read mmio_obj ;
  write mmio_obj sum ;
  spec mmio_slot (sum + x)

```

```

adder || client ≤ spec

```

What is system verification?

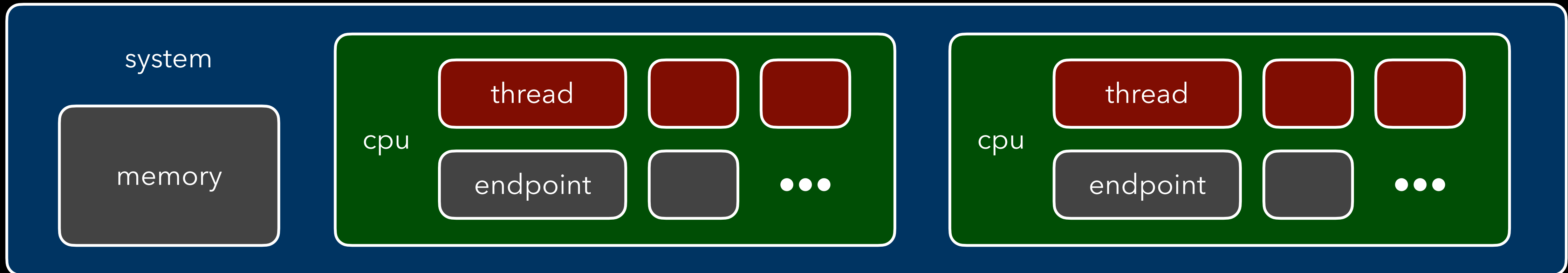
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System states

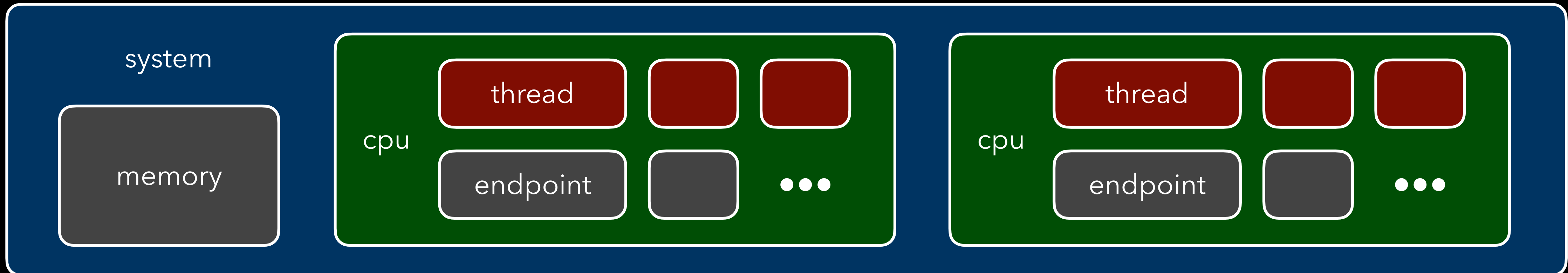


```
Record thread := {
  prog : itree thread_event void ;
  caps ...
}.
```

```
Record cpu_state := {
  threads : gmap thread_id thread ;
  endpoints ...
}.
```

```
Record system_state := {
  cpus : gmap cpu_id cpu_state ;
  memory ...
}.
```

Semantics as interaction trees



```
run_cpu (s : cpu_state) : itree cpu_event void.
```

- Interpret seL4 invocations
- Interleave thread steps
- Expose memory and I/O operations

```
run_system (s : system_state) : itree system_event void.
```

- Interpret memory operations
- Interleave CPU steps
- Expose I/O operations

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Program logic

From Iris

- Base logic
- Step indexed model
- Resource algebra library
- Ghost resources
- Invariants
- Proof mode
- ~~Language framework~~
- ~~Program logic~~

New

- Specifications as interaction trees
- Weakest-precondition program logic
- seL4-specific assertions and rules

Program logic

- Ownership assertions

- *thread-points-to*
- *endpoint-points-to*
- *slot-points-to*

$$thread_id \models_{\text{thread}} itree_program$$

$$ep_id \models_{ep} ep_state$$

$$slot_id @ thread_id \models_{\text{slot}} capability$$

- Weakest precondition assertion

- resources needed to execute safely

$$WP \ thread_id \ \{\{ \ \varphi \ \}\}$$

Program logic

Proof by symbolic execution

$\text{ep_obj} \Vdash_{\text{ep}} \text{EP_Call_Queue } [(t_{\text{client}}, x)]$

← Assume: temporary ownership of kernel objects

$\text{ep} \ @ \ t_{\text{adder}} \Vdash_{\text{slot}} \text{Cap_EP } \text{ep_obj} \ \{[\text{EP_Recv}]\}$

← Assume: ownership of capability slots

$\text{reply} \ @ \ t_{\text{adder}} \Vdash_{\text{slot}} \text{Cap_Null}$

$t_{\text{adder}} \Vdash_{\text{thread}} (r \leftarrow \text{ep_recv } \text{ep } \text{reply}; k \ r)$

← Assume: ownership of the executing program

*

$\text{WP } t_{\text{adder}} \ \{\{ \text{False} \}\}$

← Goal: prove that t_{adder} is safe to execute

Program logic

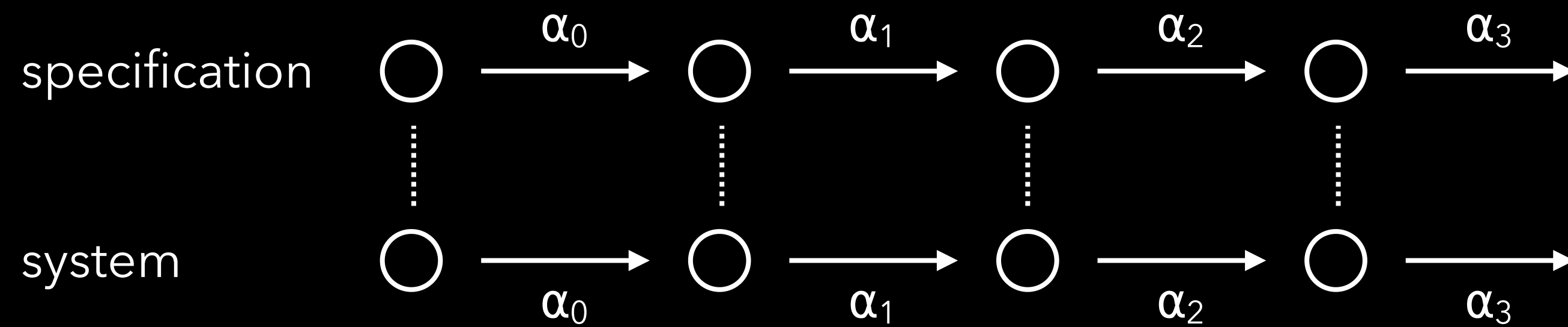
Proof by symbolic execution

$$\begin{array}{l}
 \text{ep_obj} \models_{\text{ep}} \text{EP_Call_Queue} [(\text{t}_{\text{client}}, \text{x})] \\
 \text{ep} \ @ \ \text{t}_{\text{adder}} \models_{\text{slot}} \text{Cap_EP} \ \text{ep_obj} \ \{[\text{EP_Recv}]\} \\
 \text{reply} \ @ \ \text{t}_{\text{adder}} \models_{\text{slot}} \text{Cap_Null} \\
 \text{t}_{\text{adder}} \models_{\text{thread}} (\text{r} \leftarrow \text{ep_recv} \ \text{ep} \ \text{reply}; \text{k} \ \text{r}) \\
 \hline
 \text{WP} \ \text{t}_{\text{adder}} \ \{\{ \text{False} \}\}
 \end{array}$$

$$\begin{array}{l}
 \text{ep_obj} \models_{\text{ep}} \text{EP_Idle} \\
 \text{ep} \ @ \ \text{t}_{\text{adder}} \models_{\text{slot}} \text{Cap_EP} \ \text{ep_obj} \ \{[\text{EP_Recv}]\} \\
 \text{reply} \ @ \ \text{t}_{\text{adder}} \models_{\text{slot}} \text{Cap_Reply} \ \text{t}_{\text{client}} \\
 \text{t}_{\text{adder}} \models_{\text{thread}} (\text{k} \ \text{x}) \\
 \hline
 \text{WP} \ \text{t}_{\text{adder}} \ \{\{ \text{False} \}\}
 \end{array}$$

Program logic – refinement

Every system I/O event can be matched by the specification



Program logic – refinement

Every system I/O event can be matched by the specification

- I/O specifications
 - *exclusive right to perform specified sequence of I/O operations* `io_spec itree_program`

Program logic – refinement

Every system I/O event can be matched by the specification

$\text{io_spec } (x \leftarrow \text{read } \text{mmio_obj}; k_{\text{spec}} x)$

← Assume: ownership of I/O trace specification

$\text{mmio_slot} @ t_{\text{adder}} \Rightarrow_{\text{slot}} \text{Cap_MMIO } \text{mmio_obj}$

← Assume: ownership of capability slots

$t_{\text{client}} \Rightarrow_{\text{thread}} (x \leftarrow \text{read } \text{mmio_slot}; k_{\text{client}} x)$

← Assume: ownership of the executing program

$\text{WP } t_{\text{client}} \{ \{ \text{False} \} \}$

← Goal: prove that t_{client} is safe to execute

Program logic – refinement

Every system I/O event can be matched by the specification

$$\begin{array}{l}
 \text{io_spec } (x \leftarrow \text{read mmio}_{\text{obj}}; k_{\text{spec}} \ x) \\
 \text{mmio}_{\text{slot}} @ t_{\text{adder}} \Longrightarrow_{\text{slot}} \text{Cap_MMIO mmio}_{\text{obj}} \\
 t_{\text{client}} \Longrightarrow_{\text{thread}} (x \leftarrow \text{read mmio}_{\text{slot}}; k_{\text{client}} \ x) \\
 \hline
 \text{WP } t_{\text{client}} \{\{ \text{False} \}\}
 \end{array}
 *$$

$$\begin{array}{l}
 \text{io_spec } (k_{\text{spec}} \ x) \\
 \text{mmio} @ t_{\text{adder}} \Longrightarrow_{\text{slot}} \text{Cap_MMIO mmio}_{\text{obj}} \\
 t_{\text{client}} \Longrightarrow_{\text{thread}} (k_{\text{client}} \ x) \\
 \hline
 \text{WP } t_{\text{client}} \{\{ \text{False} \}\}
 \end{array}
 *$$

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Conclusion

- Status
 - Implementing semantics and logic for a simplified model of seL4
- Topics for another talk
 - Reasoning about shared resources using invariants and ghost resources
 - Robustness: proving properties in the presence of untrusted apps
 - Nondeterminism and failure
- Scalability
 - Requires modularity, compositionality, abstraction



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