

DeepComputing



Porting seL4 to the RISC-V SoC, toward a Secure and High-Performance RISC-V AI Platform

Aug 2025

Yuning Liang

Founder

a core software guy

Java VM (J2ME)

Static Compiler/Analysis (MIPS' Open64)

People who are really
serious about
software should make
their own hardware.

Alan Kay

Deep Computing



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Who are we and What we do

RISC-V Premium Product Pioneer Focusing on

- Consumer Electronics
- Modern Personal Computing Devices
- And Some RISC-V Run & Fun Gadgets



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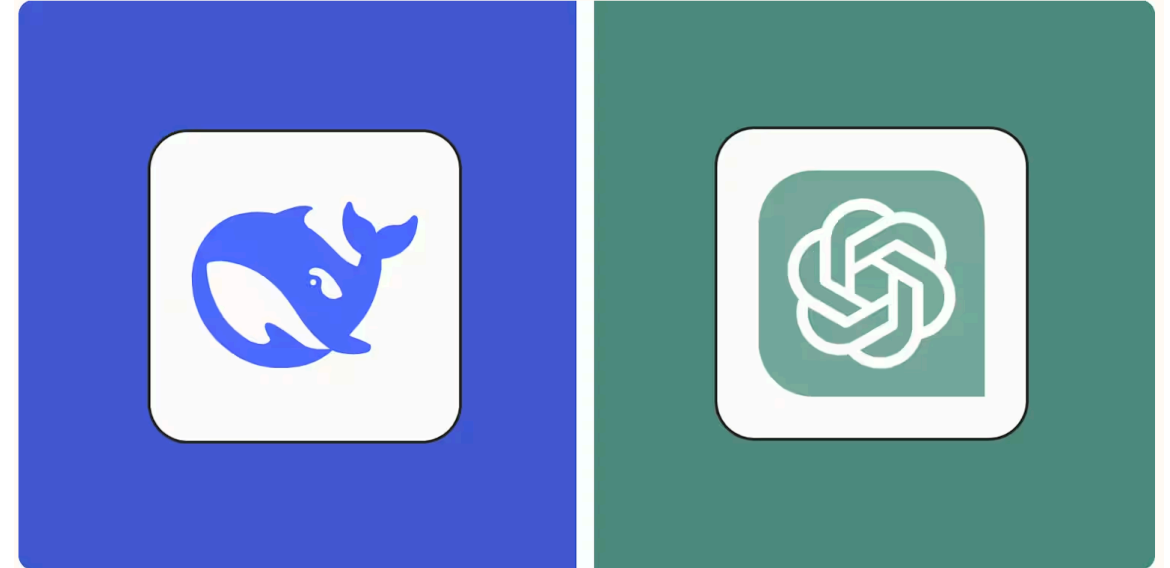
Surge of AI, DeepSeek vs ChatGPT

Where we are now:

- Lower Compute Cost
- Faster Inferencing and Training

What we can do on Local Device

- Single Inferencing for Distill Models
- Multi Local Device Inferencing and Post Train Over Full-Blood Models



AI PC For RISC-V

2024 Start Partnering Linux OS

- Linux Kernel Fellow
- Ubuntu Official Support
 - 25.10 for < RVA23
 - 26.04 for > RVA23
- Fedora Official Support
 - 47 for > RVA23



Fedora Progress

- **Fedora** is a community Linux distribution project
- **Fedora Remix** program provides branding for Fedora for specific hardware, supported by the creator & the Fedora community
- Strong focus on contributing back **upstream**
- **Framework** laptops already part of Fedora Ready, RISC-V is a fantastic addition to supported platforms
- Congratulations & deep respect to **DeepComputing** for their Fedora Lab!

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Jeffrey Osier-Mixon
Elected RISC-V Strategic Board Member,
Red Hat/IBM

fedora remix **fedora**

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A photograph of a man on a stage with a large RISC-V logo in the background.

A photograph of Gordan Markus on a stage, wearing a dark jacket with a logo.

RISC-V @ Ubuntu Summit

RISC-V is all about collaboration!

Last year @ Ubuntu Summit

- Presentation by John Ronco, SiFive

This year @ Ubuntu Summit

- Presentation by Yuning Liang, DeepComputing
- Pioneers in creating RISC-V consumer devices
- Enabling RISC-V to reach the developer community in familiar form factors
- Exactly what the RISC-V ecosystem needed!

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Gordan Markus
Director Silicon Alliances,
Canonical

Canonical

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Challenges Faced for RISC-V SoC

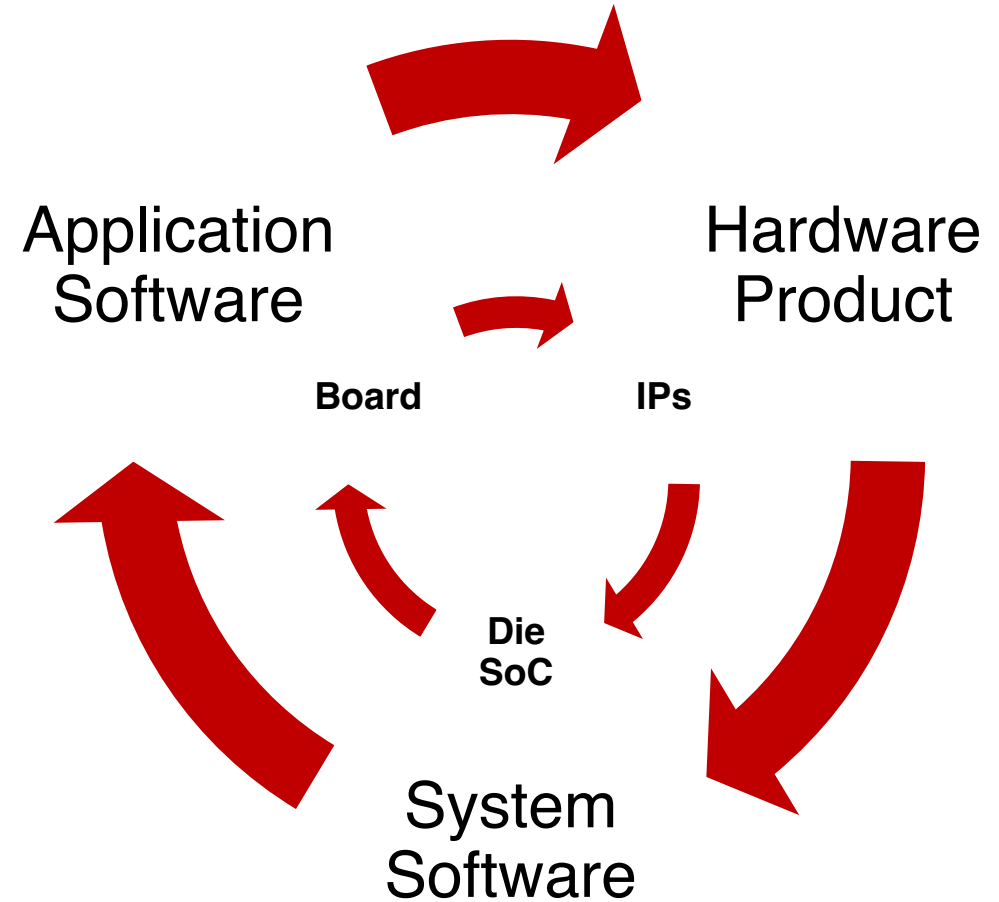
- **Unknown Target Market**
- **Unknown Required Compute Power**
- **Limited Resource Constraint**
- **Limited Time Constraint**
- **Time to All in AI?**

Long Painful Journey Towards Mass Production

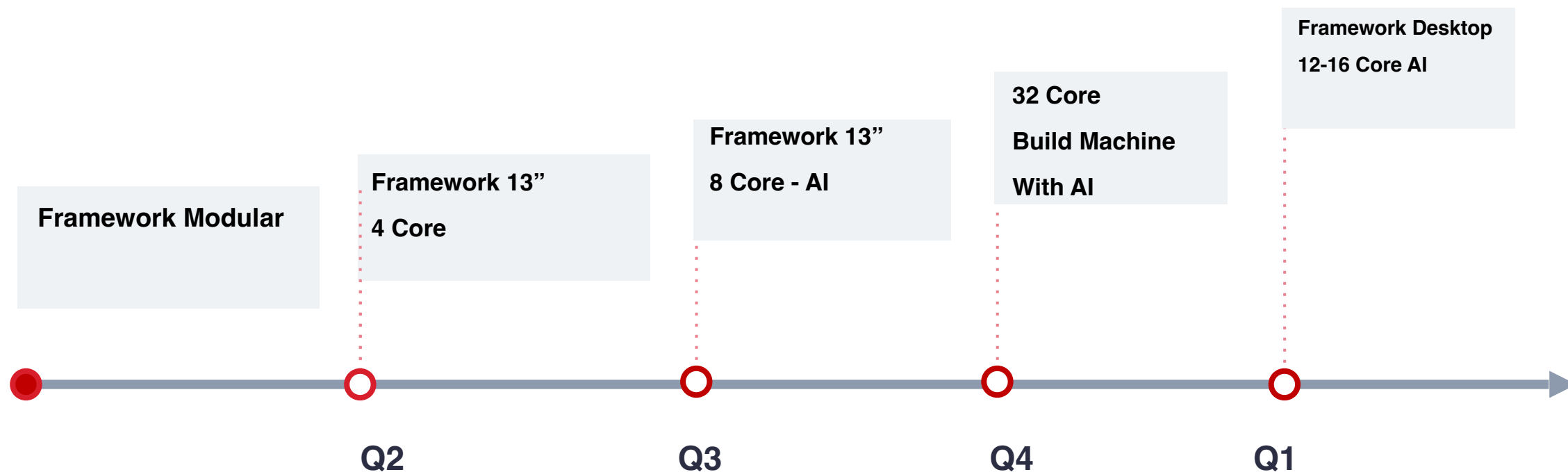
A full development cycle for
high end SoC

from IP to SoC, Board
System Software, Application,
to a mass produced end user product,

takes 5-7 years!!!

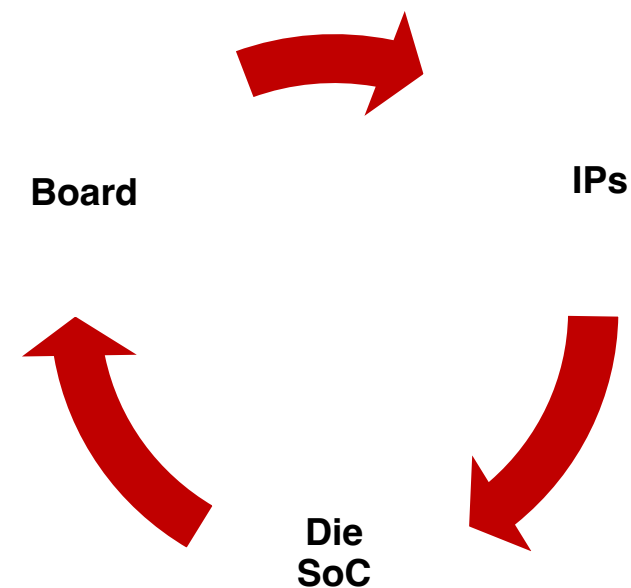


Exciting 2025-2026 Roadmap

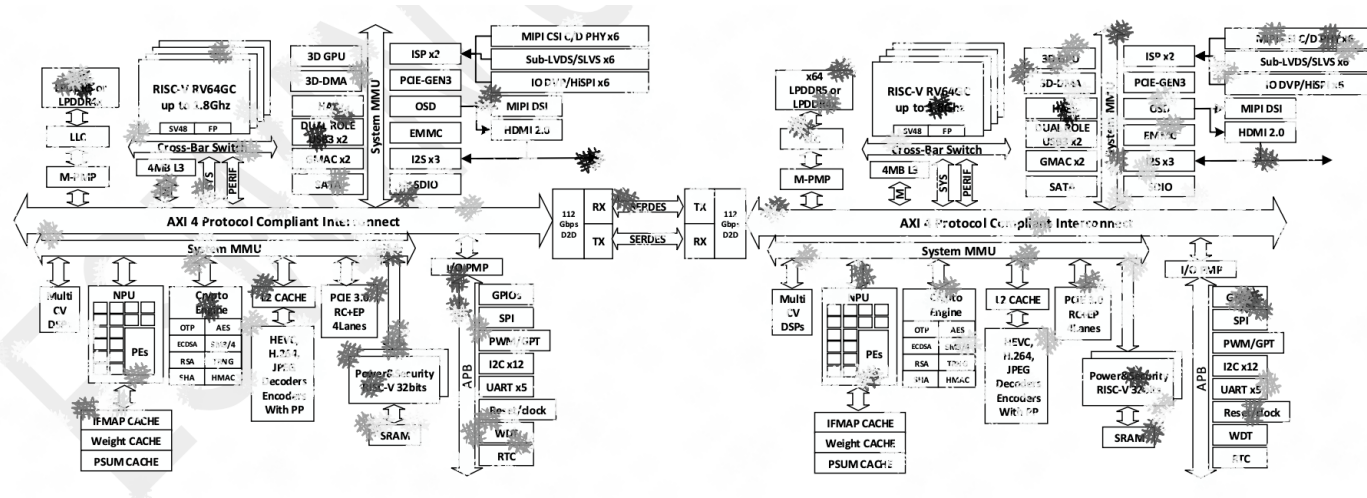


Flexibility for Making RISC-V AI a Successful Reality

- Prepare for the Future Unknown
 - A Retro-fit Lego like Approach
 - Standard Interface on All Levels
 - Modular at all time
-
- **IP/Die: Chiplet**
 - **Die/SoC: PCIe Host/Device**
 - **SoC/Board: Type-C**
 - **What Else? End Product Level**



Chiptlet Solution: an ESWIN 7702



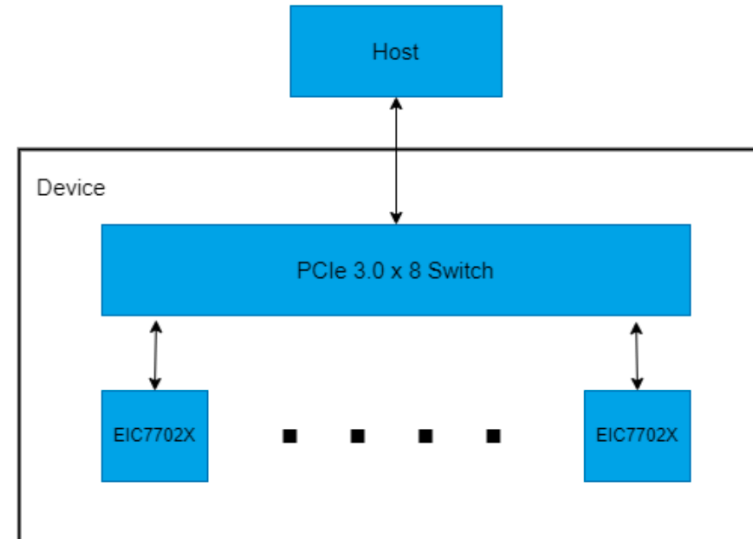
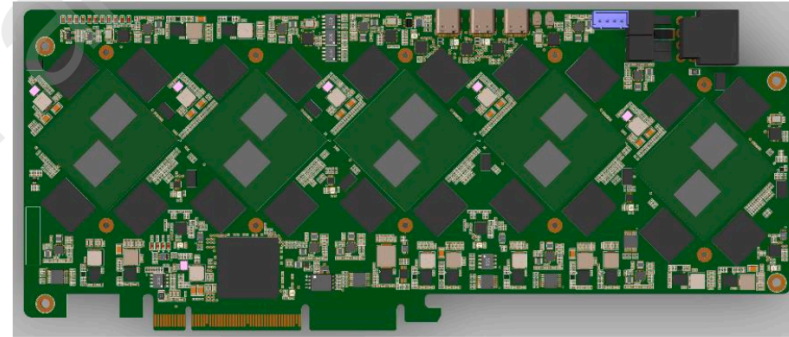
First RISC-V Chiptlet AI SoC in the world.

- Chiptlet 2-DIE, 2GHz 8-Core.
- 64G LPDDR5
- 50 TOPS AI (NPU+GPU+CPU)
- 8K@50fps Encoding
- RVV 1.0 on DSP


PCIE Solution: An example: ESWIN 7702X

First RISC-V Chiplet AI SoC in the world.

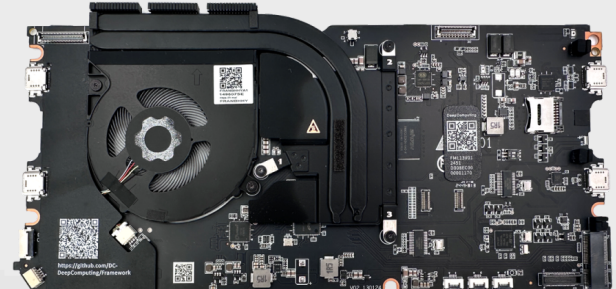
- First RISC-V Chiplet AI SoC in the world with PCIE HOST and DEVICE support simultaneously.
- Ethernet Over PCIE




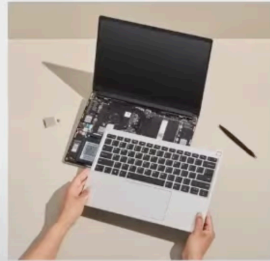
Framework RISC-V AI-PC Product Portfolio



DeepComputing x Framework

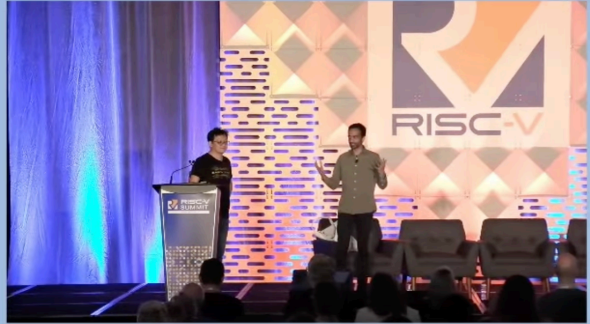



Nirav Patel
CEO
 framework



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NORTH AMERICA

DeepComputing x Framework Partnership

DeepComputing

Framework RISC-V AI-PC Product Portfolio



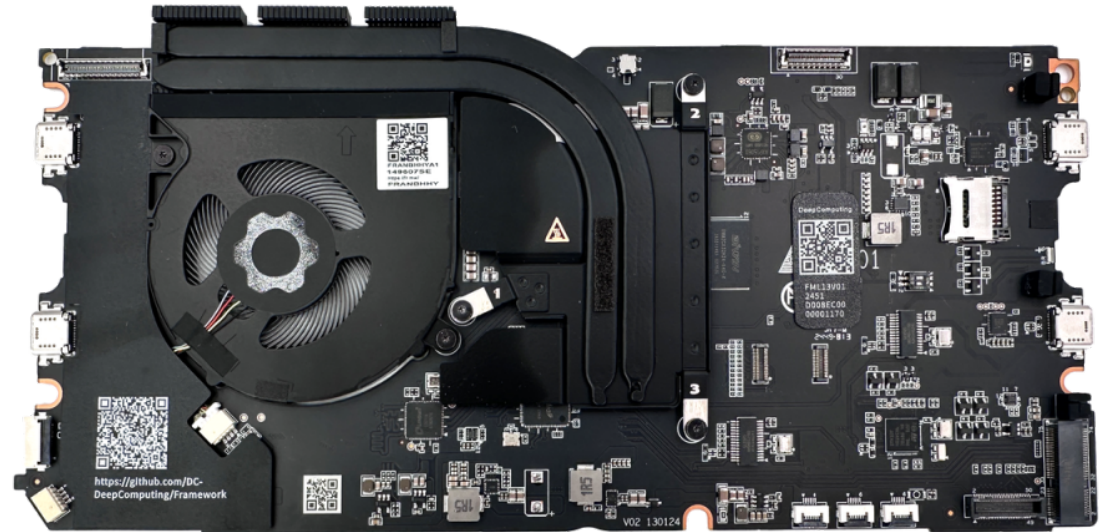
Desktop and Laptop 12"/13"/16"

Framework RISC-V AI-PC Product Portfolio



Laptop 13" RISC-V

- 8 Core 2GHz, 128G LPDDR5+
- 50 TOPS AI Local Compute
- **June, \$300+**



Framework RISC-V AI-PC Product Portfolio



Framework 16" RISC-V Extension

- 8 Core 2GHz, 128G LPDDR5
- 100 TOPS AI Local Compute
- Q3, \$300+



Framework 16" Extension Example ONLY

Framework RISC-V AI-PC Product Portfolio



Desktop RISC-V

- 16 Core 2GHz, <256G LPDDR5+
- 100 TOPS AI Local Compute
- Q4, \$700+



So Far SeL4 Progress on RISC-V

- No Virtualisation until RVA23 in 2026
- Not likely seeing any current SeL4 application fully ported
 - Automotive (Horizon, Nio, Li Auto)
 - SeL4 + Linux
 - AI Box (any idea?)
 - SeL4 + LLM

ESWIN Platform

1. OpenSBI → Uboot Booting, OK!
2. SeL4Test
 - Image and dtb → OK!
 - Loading → OK!
 - Running → Not OK! Minor Failure on Timer, TIMER0001
3. SeL4 Kernel, some Random Crashing!
 - Need some body help cracking on.

RISC-V Autonomous Platform



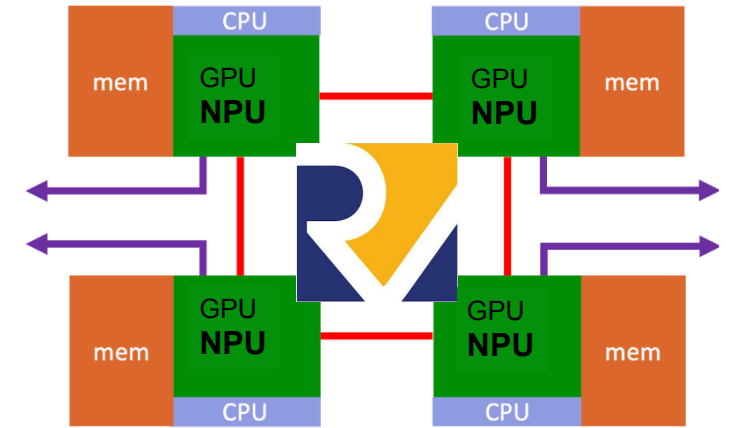
Horizon J5 + ARM RK 3588

→ Horizon J5 + RISC-V ESWIN 7702X



AI BOX Platform

1. 4 x ESWIN 7702 SoC Chiplet
 - PCIE Ring Topology
 - 4GB/s upstream, 4GB/s downstream
 - 4 x (8-core CPU/NPU/GPU), 200 TOPS
 - 256G DDR
 - <200B LLM models @ 10 Token/S
2. Unlimited node ring expansion
 - 4 x Board, DeekSeek 671B
 - Any Idea on applying SeL4?





100

Open Community Project RISC-V Sponsorship

- **1000** New Contributors Awareness and RISC-V Membership
- **100** Excellent RISC-V Contributors

Sponsorship

RISC-V + Framework

- **Free Framework Devices**
- **Award** for Excellent Contribution
- **Speeches Opportunities on RISC-V Summit and Workshop**





100 AI Startups RISC-V Sponsorship

- **1000** New AI Contributors Awareness and RISC-V Membership
- **100** Excellent RISC-V AI Contributors

Sponsorship

RISC-V + Framework + AI Accelerator

- **Free Framework Devices with AI Compute**
- **Award** for Excellent Contribution
- **Speeches Opportunities on RISC-V Summit and Workshop**



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Thank You



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