

# Model-based Development for seL4 Microkit/Rust with Integrated Formal Methods using HAMR

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seL4 Summit – Sept 3, 2025

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*With collaborators at ...*

Collins Aerospace

Dornerworks

UNSW

Proofcraft

Carnegie Mellow Univ.

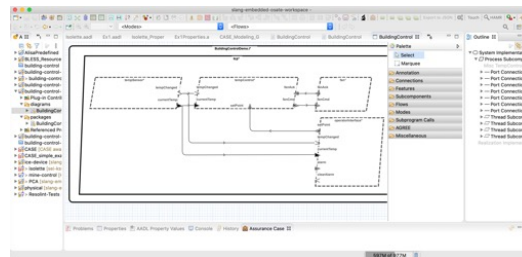
Univ. of Kansas

HAMR - SysMLv2/AADL to Rust + seL4

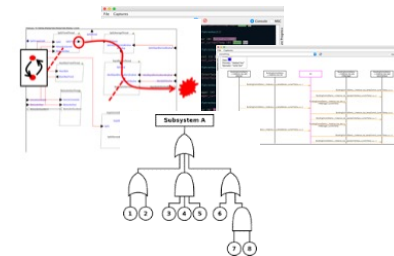
# HAMR

**HAMR** – tool chain for [H]igh [A]ssurance [M]odeling and [R]apid engineering for embedded systems

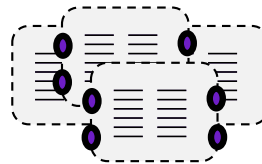
Modeling, analysis, and verification in the **SysMLv2** and **AADL** modeling languages



*Model-level behavior specifications  
(e.g., contracts) and analyses*



Component development, automated testing, and verification in multiple languages



- C
- Rust with Verus verification
- Slang (developed at Kansas State)
  - safety-critical subset of Scala
  - contract-based verification
  - transpiles to C and Rust

Deployments aligned with AADL run-time on multiple platforms

JVM Deployment



Linux Deployment



seL4 Deployment



Camkes & microKit

HAMR - SysMLv2/AADL to Rust + seL4

# Potential Benefits to seL4 Application Developers

**A systems engineering environment** based on standardized modeling languages (SysMLv2, AADL) with accompanying analysis, verification, and assurance case tools

Industrial workflows

Requirements Engineering

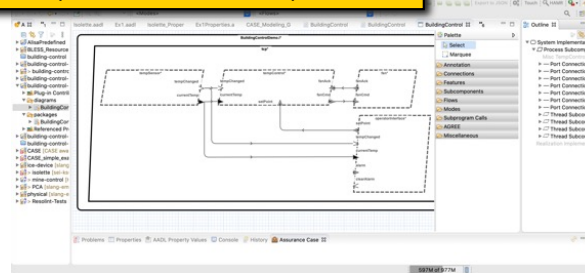
Planning Diagrams



Domain Concepts

Systems Engineering

SysMLv2 / AADL IDE – VSCode / Cameo

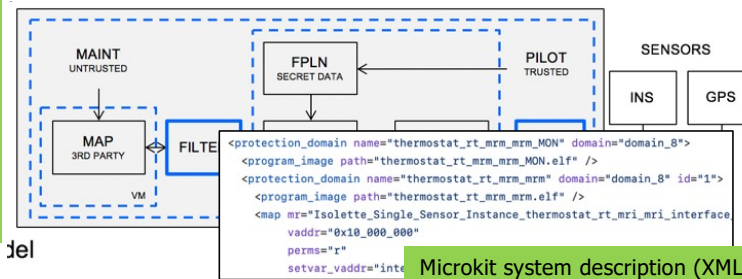


..integrate seL4 configuration with...

Software/Hardware/Middleware modeling  
Architecture constraints / patterns  
Component contracts + verification  
Assurance case construction  
..  
Information Flow Spec & Analysis  
Timing / Scheduleability

Microkit / CAMKES Specification

seL4 Deployment

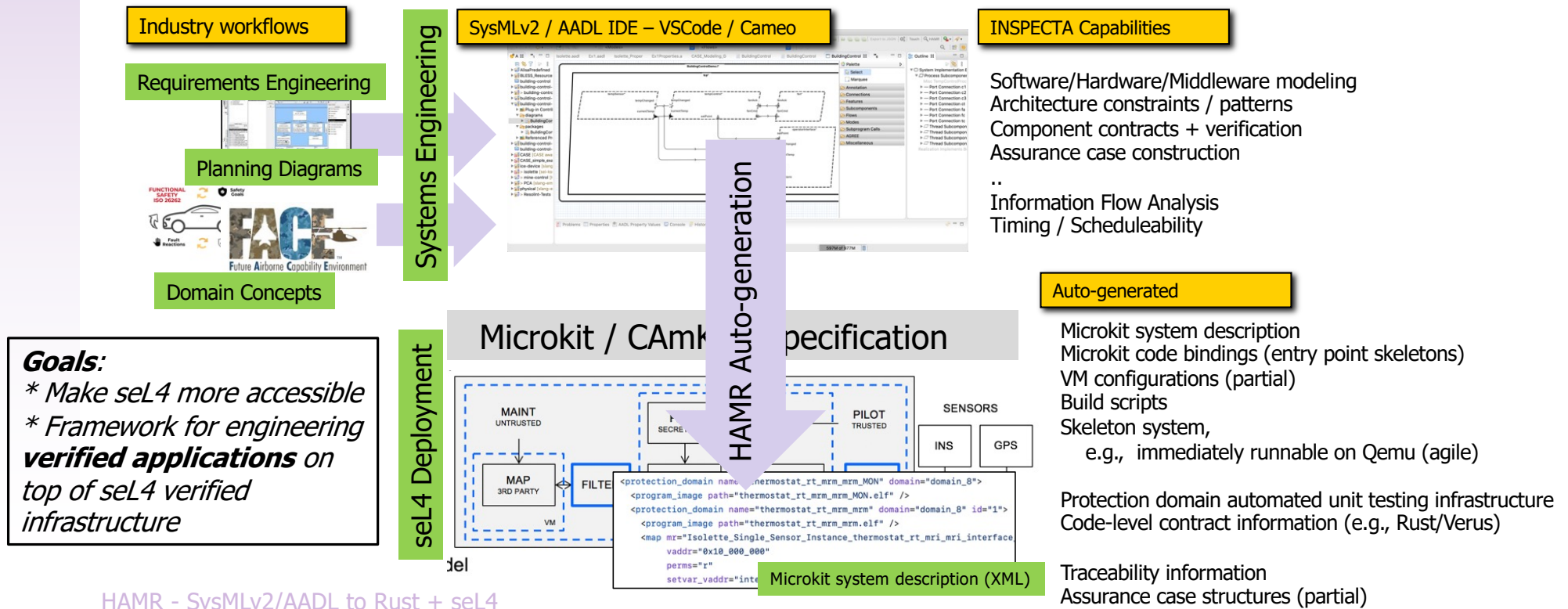


Existing seL4 ecosystem tools for  
component-oriented specification of  
seL4 capabilities,  
partitioning, and  
inter-partition communication

HAMR - SysMLv2/AADL to Rust + seL4

# Potential Benefits to seL4 Application Developers

**A systems engineering environment** based on standardized modeling languages (SysMLv2, AADL) with accompanying analysis, verification, and assurance case tools



# Context and Target Applications

On the DARPA PROVERS program, HAMR is being used to develop an experimental version of the mission computer for the Collins "**Launched Effects**" platform (final development will emphasize HAMR SysMLv2 to Rust)



Launched Effects **Mission Computer**



**..increase security and modularity**

**..decrease costs** for development and assurance

Video: <https://youtu.be/SwPJHmZQMaM?si=NwTdb3VFpV-MxSre>

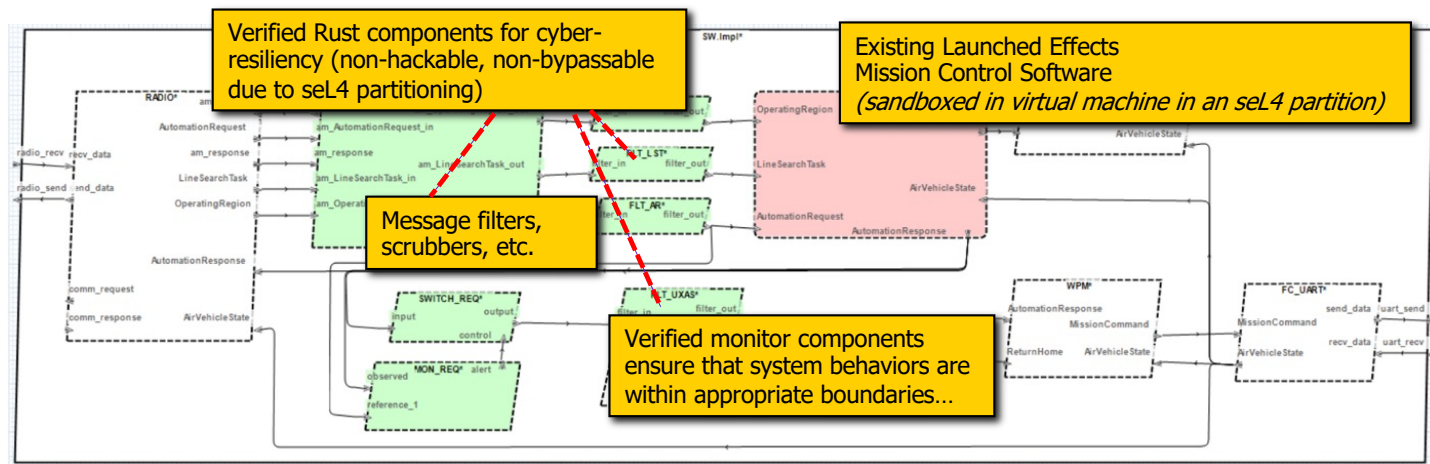
*DARPA PROVERS*  
= "integrating pipelines of formal methods in defense industry development processes"



HAMR - SysMLv2/AADL to Rust + seL4

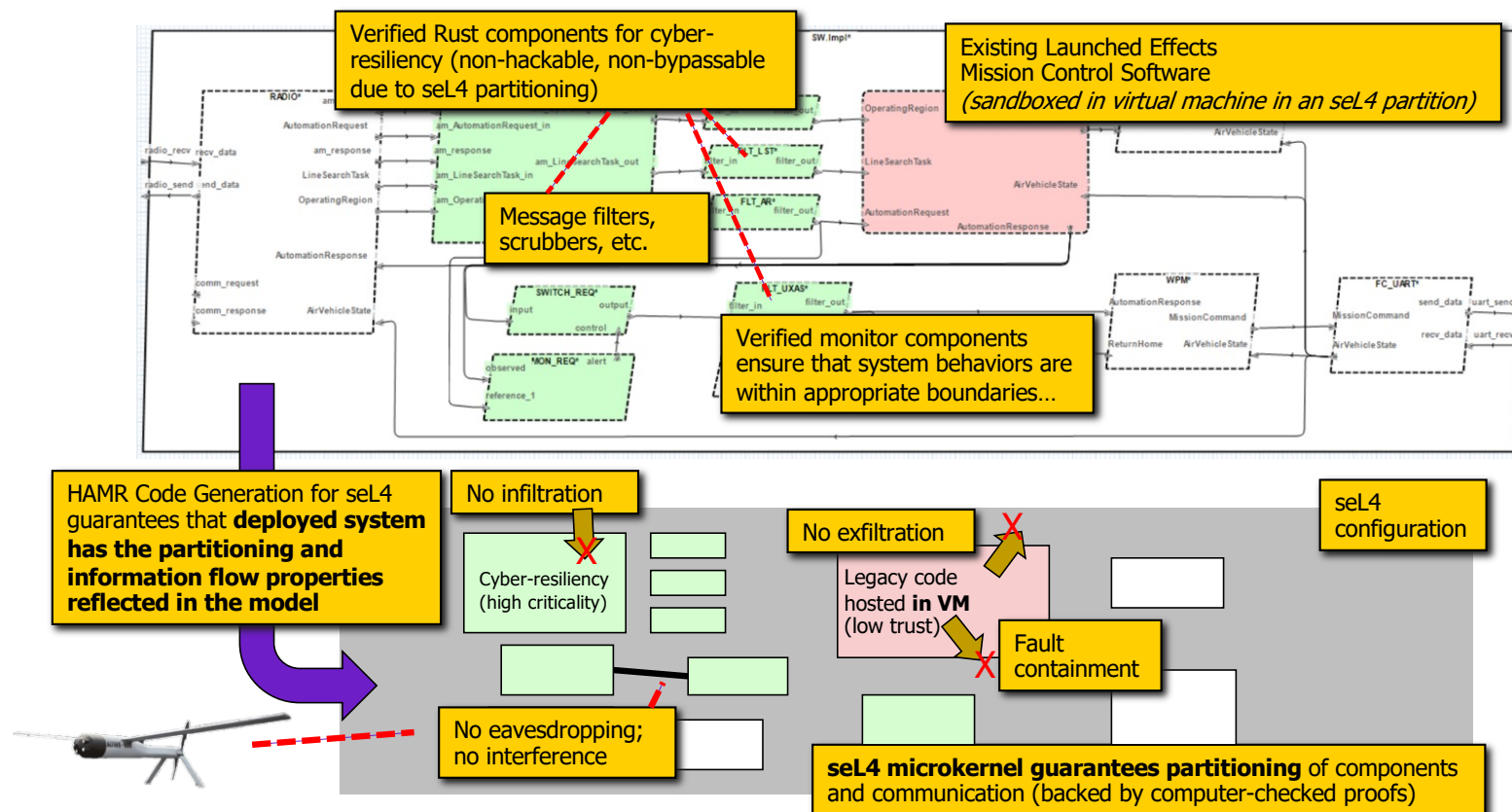
# Characteristics of Supported Systems

Use HAMR SysMLv2/AADL modeling to specify partitioning, communication architecture of improved system



# Characteristics of Supported Systems

Use HAMR SysMLv2/AADL modeling to specify partitioning, communication architecture of improved system



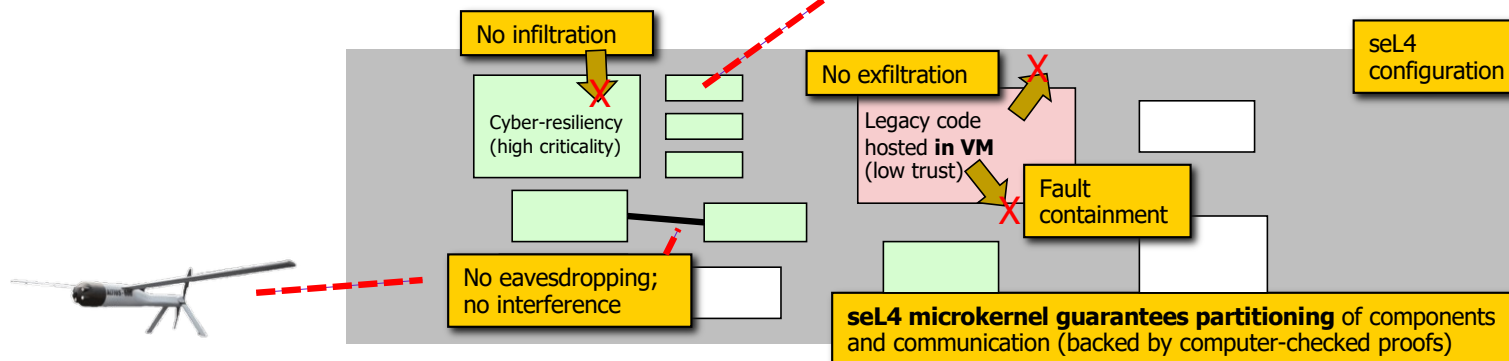
HAMR - SysMLv2/AADL to Rust + seL4

# Verified Component Code

PROVERS program  
emphasis on memory  
safe languages...

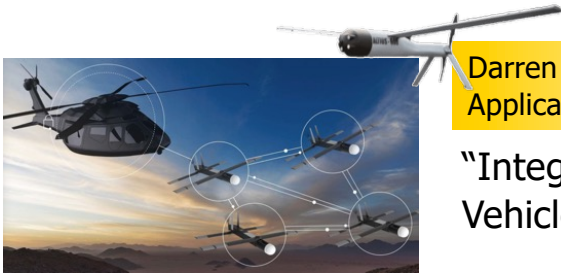
Rust (with Verus verification)

INSPECTA Focus



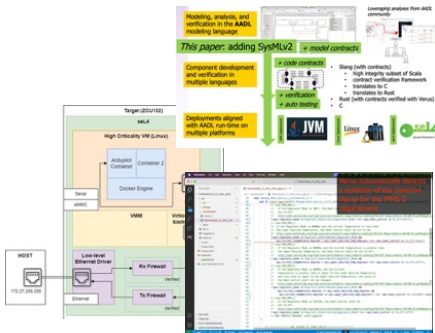
HAMR - SysMLv2/AADL to Rust + seL4

# Other Summit INSPECTA-Related Talks



Darren Cofer (Principal Investigator) –  
Application to Collins Launched Effects

“Integration of seL4 in a Flight  
Vehicle Mission System”



Robert VanVossen –  
Rust contract-based development, testing,  
and verification of firewall components

“Rust-based drivers and verified rust  
applications on seL4”

Gerwin Klein –  
Automating seL4 kernel correctness proofs  
for new platforms

“The next 700 verified seL4  
platforms”

Gernot Heiser –  
Verified infrastructure and services

“Trustworthy Systems R&D Update”

Junming Zhao –  
Verified infrastructure and services

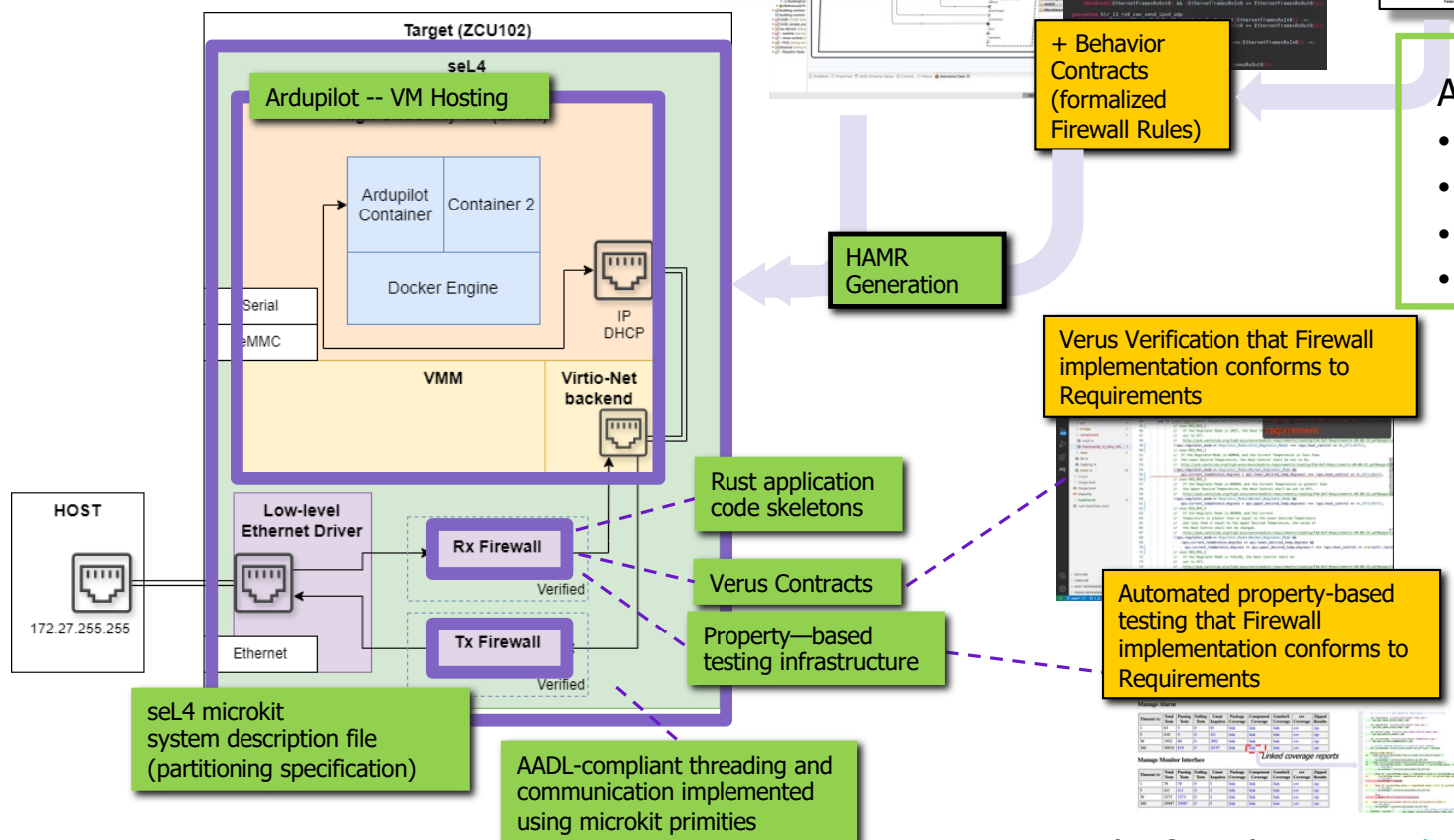
“Verifying Device Drivers with Pancake”

# Robert Vanvossen Talk

## Dornerworks

"Rust-based drivers and verified rust applications on seL4" -- *Thursday*

## INSPECTA – Public Demonstrator Example



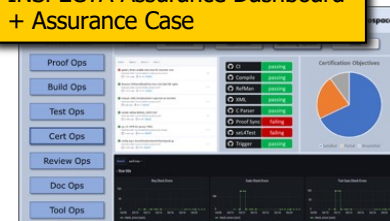
## Firewall Requirements (natural language)

*Recent demo!*

## Automated..

- metrics generation
- traceability info
- attestation (w/ KU)
- assurance case evidence

## Verus Verification that Firewall implementation conforms to Requirements

INSPECTA Assurance Dashboard  
+ Assurance Case

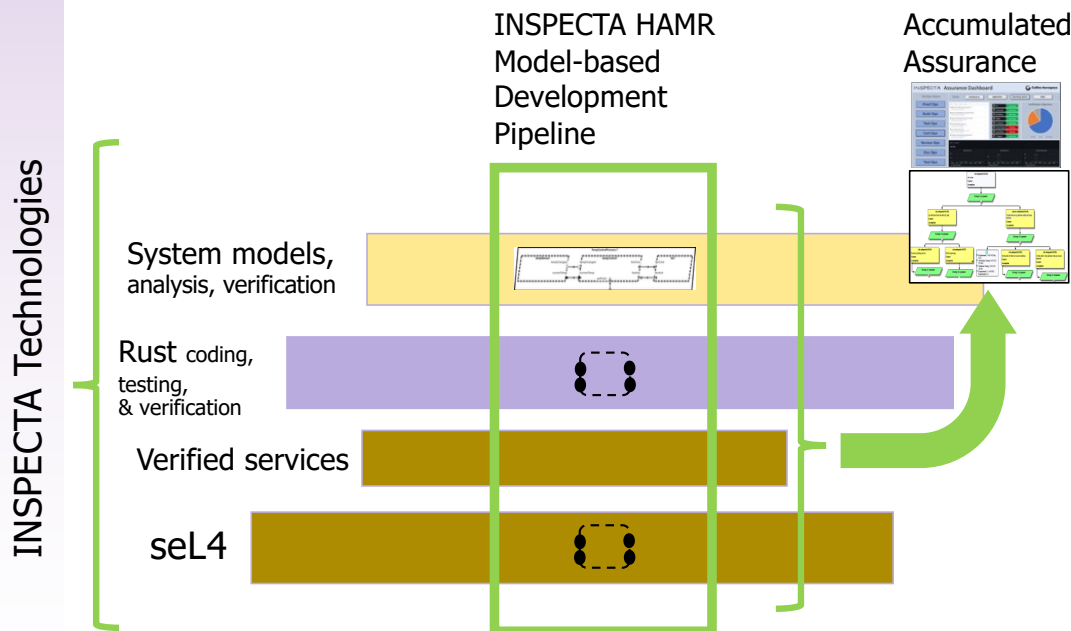
## Automated property-based testing that Firewall implementation conforms to Requirements

...Dornerworks found a **10x reduction** in development time.

HAMR - SysMLv2/AADL to Rust + seL4

# INSPECTA “PROVERS Pipeline” Scope

A primary goal of PROVERS is to demonstrate “pipelines” of formal methods capabilities. Designing and managing the INSPECTA “pipeline” entails a lot of extra work...



*To fully demonstrate pipeline concepts within program timeline, the scope of the pipeline needs to be narrower than that of the individual technologies*

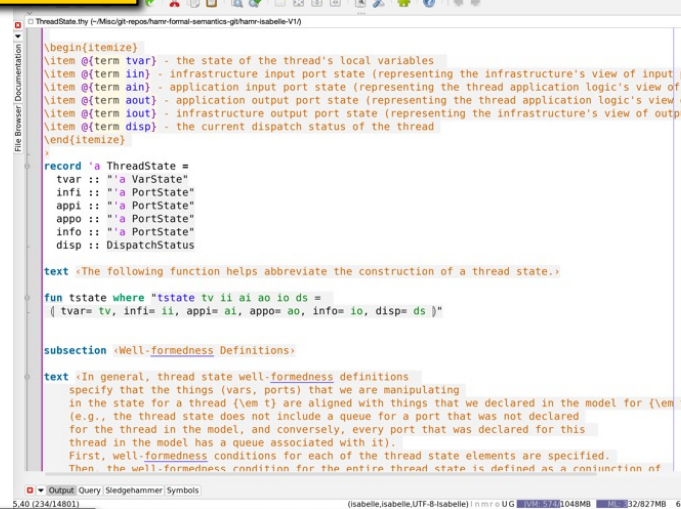
- Interactions across the pipelines stages are organized a **core** set of computational and data **abstractions** that are amenable to **formal verification**
- **Semantics** of these abstractions must be maintained and **traceable across the stages**
- Claims, contributions of stages, and assurance evidence must be accumulated across the stages

HAMR - SysMLv2/AADL to Rust + seL4

# HAMR Formal Semantics for INSPECTA Pipeline

150+ page literate-style Isabelle/HOL theories for AADL/SysMLv2 HAMR execution model (guides our design of our contracts and verification/testing framework)

Isabelle



```
(begin(itemize))
\item @term tvar - the state of the thread's local variables
\item @term in - infrastructure input port state (representing the infrastructure's view of input p
\item @term ain - application input port state (representing the thread application logic's view of
\item @term out - application output port state (representing the thread application logic's view of
\item @term iout - infrastructure output port state (representing the infrastructure's view of output
\item @term disp - the current dispatch status of the thread
\end(itemize))

record 'a ThreadState =
  tvar :: "'a VarState"
  in :: "'a PortState"
  ain :: "'a PortState"
  appo :: "'a PortState"
  info :: "'a PortState"
  disp :: DispatchStatus

text <The following function helps abbreviate the construction of a thread state.>

fun tstate where "tstate tv ii ai ao io ds =
  { tvar= tv, in= ii, ain= ai, appo= ao, info= io, disp= ds }"

subsection <Well-formedness Definitions>

text <In general, thread state well-formedness definitions
specify that the things (vars, ports) that we are manipulating
in the state for a thread (vem t) are aligned with things that we declared in the model for {vem t}
(e.g., the thread state does not include a queue for a port that was not declared
for the thread in the model, and conversely, every port that was declared for this
thread in the model has a queue associated with it).
First, well-formedness conditions for each of the thread state elements are specified.
Then, the well-formedness condition for the entire thread state is defined as a conjunction of
```

Latex/PDF generated from Isabelle

Joint work with  
Stefan Hallerstede  
(U. Aarhus)

record 'a ThreadState =  
 tvar :: 'a VarState  
 in :: 'a PortState  
 ain :: 'a PortState  
 appo :: 'a PortState  
 info :: 'a PortState  
 disp :: DispatchStatus

The following function helps abbreviate the construction of a thread state.

fun tstate where "tstate tv ii ai ao io ds =  
 { tvar= tv, in= ii, ain= ai, appo= ao, info= io, disp= ds }"

### 2.4.2 Well-formedness Definitions

In general, thread state well-formedness definitions specify that the things (vars, ports) that we are manipulating in the state for a thread  $t$  are aligned with things that we declared in the model for  $t$ . (e.g., the thread state does not include a queue for a port that was not declared for the thread in the model, and conversely, every port that was declared for this thread in the model has a queue associated with it). First, well-formedness conditions for each of the thread state elements are specified. Then, the well-formedness condition for the entire thread state is defined as a conjunction of these properties.

#### Well-formed Thread State Elements

definition wf-ThreadState-tvar:: Model  $\Rightarrow$  CompId  $\Rightarrow$  ('a VarState)  $\Rightarrow$  bool where  
 wf-ThreadState-tvar m c vs  $\equiv$  wf-VarState vs {v . isVarOfCID m c v}

The in component of a ThreadState (input infrastructure port map) is well formed when the domain of the in port map is equal to the set of input ports for the thread declared in the model. Intuitively, each of the declared "in" ports for the thread (according to the model) is associated with an infrastructure message queue, (and there are no "extra" ports in the map).

definition wf-ThreadState-infi:: Model  $\Rightarrow$  CompId  $\Rightarrow$  ('a PortState)  $\Rightarrow$  bool where  
 wf-ThreadState-infi m c ps  $\equiv$  wf-PortState ps {p . isInCIDPID m c p}

The definitions below for other port-state elements are similar.

definition wf-ThreadState-appi:: Model  $\Rightarrow$  CompId  $\Rightarrow$  ('a PortState)  $\Rightarrow$  bool where  
 wf-ThreadState-appi m c ps  $\equiv$  wf-PortState ps {p . isInCIDPID m c p}

definition wf-ThreadState-appo:: Model  $\Rightarrow$  CompId  $\Rightarrow$  ('a PortState)  $\Rightarrow$  bool where  
 wf-ThreadState-appo m c ps  $\equiv$  wf-PortState ps {p . isOutCIDPID m c p}

definition wf-ThreadState-info:: Model  $\Rightarrow$  CompId  $\Rightarrow$  ('a PortState)  $\Rightarrow$  bool where  
 wf-ThreadState-info m c ps  $\equiv$  wf-PortState ps {p . isOutCIDPID m c p}

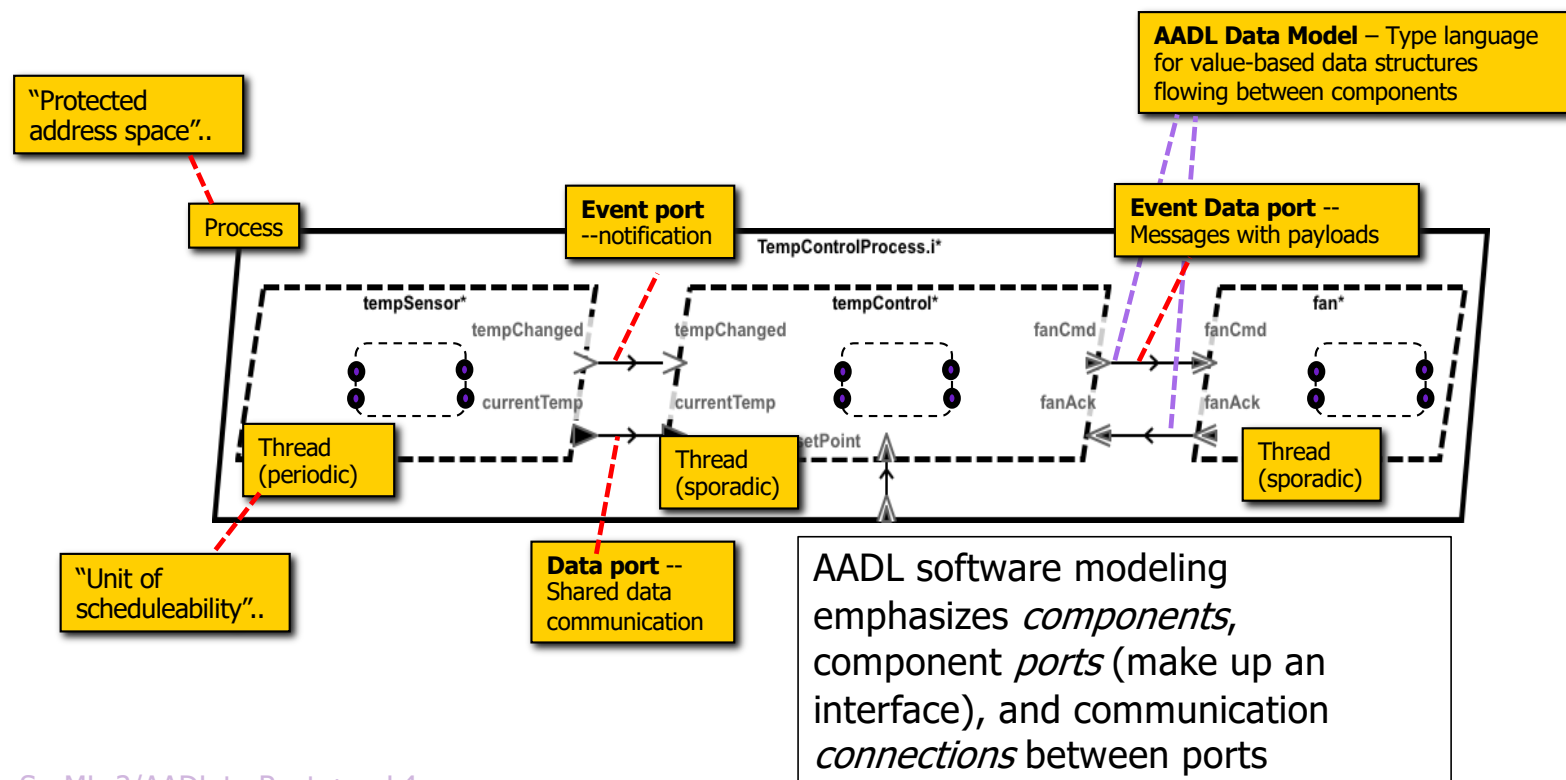
## PROVERS

- Enhanced and scope expanded
- Prove soundness of contract framework
- Extend formalization downwards towards sel4 proof-base

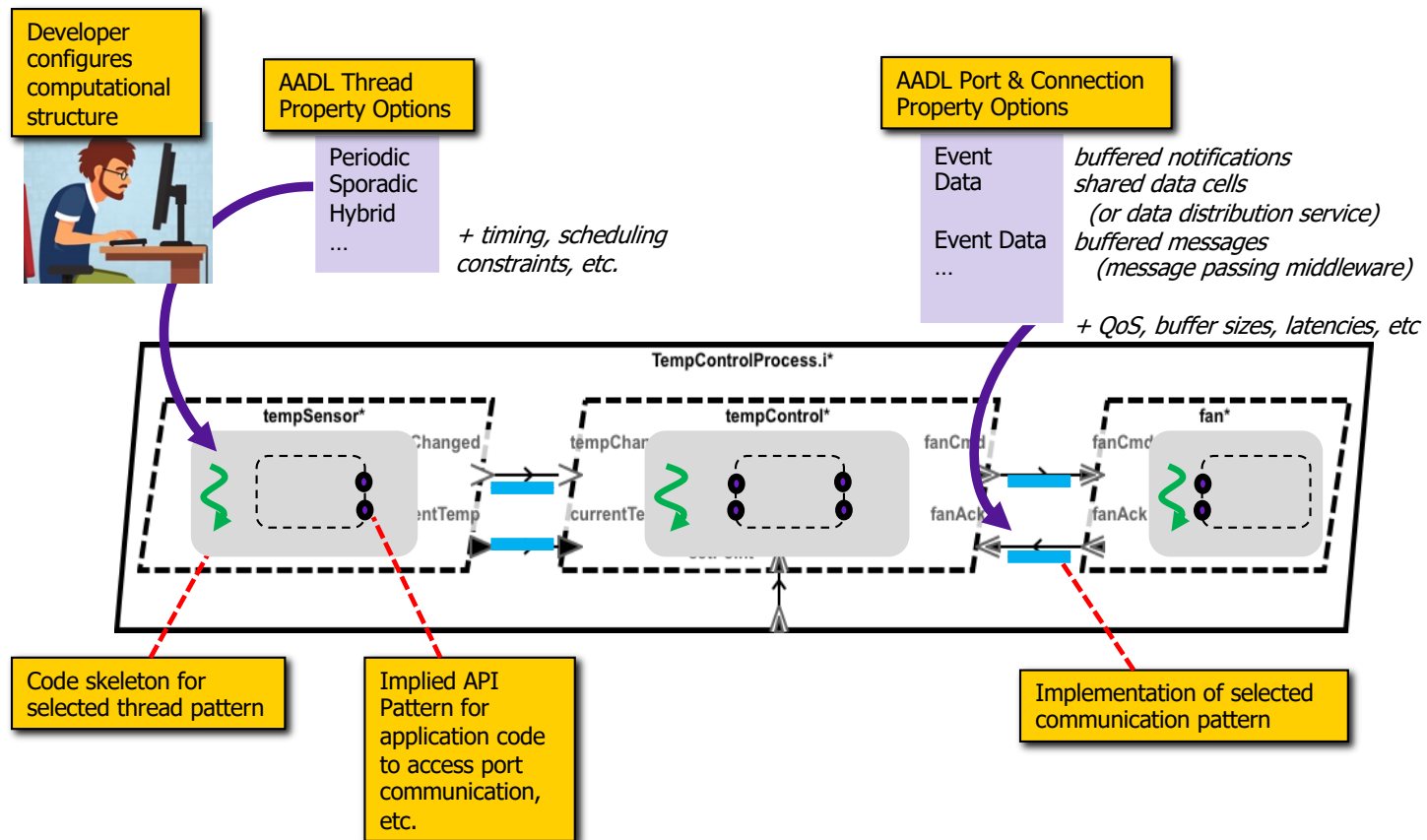
Note: limited scope: HAMR subset of AADL/SysMLv2; run-time semantics; connection to code generator by manual inspection

# AADL Modeling Concepts

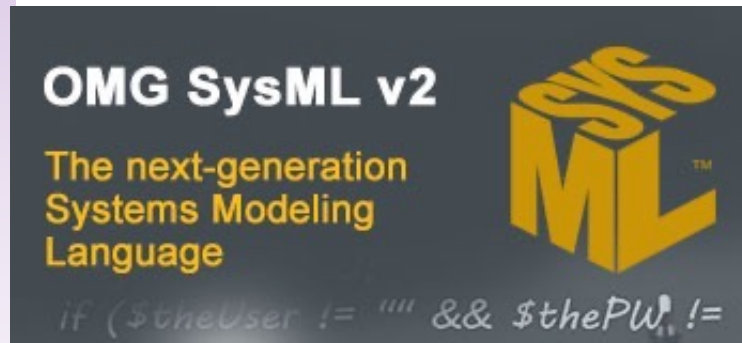
Each AADL modeling element is classified according to its role in embedded system architecture...



# AADL Modeling Concepts




# AADL to SysMLv2




*Why might SysMLv2 provide a alternate vehicle for rigorous model-based development, including AADL concepts?*

- Like AADL, has both a graphical view and textual view
- Many AADL modeling elements have analogues in SysMLv2
  - E.g., components, ports, connections, developer-defined attributes
- Aims to provide a stronger “semantics” for system engineering compared to UML, SysMLv1
- Re-engineered from the ground up
  - No backwards compatibility with SysMLv1 except through translation
  - Not built as a profile of UML
- Will have wide-ranging commercial tool support as well as open source implementations

# Standardization Effort - Migrating AADL to SysMLv2



## About the SMC



The OMG Systems Modeling Community gathers people interested in advancing SysMLv2

Different membership structure

See <https://www.omg.org/communities/>

RTESC Workgroup – entity responsible for integrating AADL concepts into SysMLv2

Charter: *"Develop domain libraries w/ KerML & SysMLv2 to support the precise modeling of Real-Time Embedded Safety-Critical Systems. Integrate capabilities from domain-specific models like SAE AADL, OpenGroup FACE, OMG MARTE, & AutoSAR"*

Lead: Gene Shreve (i3-Corp), Jerome Hugues (CMU/SEI)

4

AADLv2 / SysMLv2 review

RTESC WG

- Working with OMG RTESC working group to prototype AADL concepts in SysMLv2
- We are one of the most active participants working on building end-to-end tools for formal methods and code generation
- "Trail blazers" on integrating formal contract languages in SysMLv2 IDE

# VSCoDe SysMLv2 HAMR Front End

We developed a VSCode SysMLv2 HAMR front-end based on the SysIDE VSCode plug-in

*SysMLv2  
component  
interfaces*

*Code-level  
artifacts in  
same IDE:  
Integration of  
MicroKit-based  
Slang, Rust and  
C development  
for seL4*

*AADL Library Properties as  
SysMLv2 attributes*

*SysMLv2 encodings of  
datatypes specified  
using AADL Data  
Modeling Language*

*Formal behavior  
specifications in  
GUMBO contract  
language*

*Verification results for  
model-level contracts*

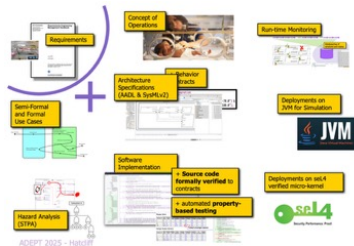
SysMLv2/AADL for HAMR with seL4 Microkit

# Artifacts & Workflow -- Detailed Technical Report

## Isolette – Infant Incubator



- *9 Real-time Tasks*
- *~40 component-level requirements*
- *Interestesting modal behavior*



### End-to-end Artifacts

- ConOps
- Use Cases
- Requirements
- Models
- Contracts
- Testing
- Verification
- Assurance Case

## The Isolette System: Illustrating End-to-End Artifacts for Rigorous Model-based Engineering

(Collins Aerospace INSPECTA Technical Report)

John Hatcliff and Jason Belt

The Isolette System: Illustrating End-to-End Artifacts for Rigorous Model-based Engineering (Collins Aerospace INSPECTA Technical Report) .....

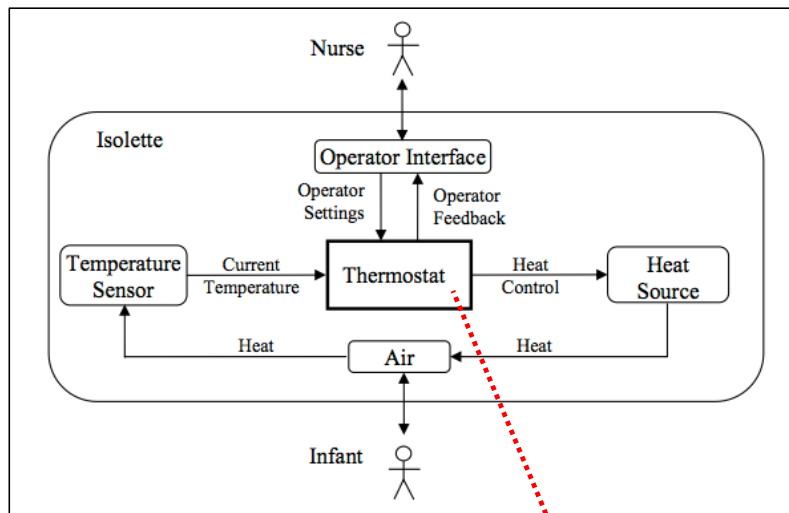
John Hatcliff and Jason Belt	
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50+ page report w/  
Git repo and videos

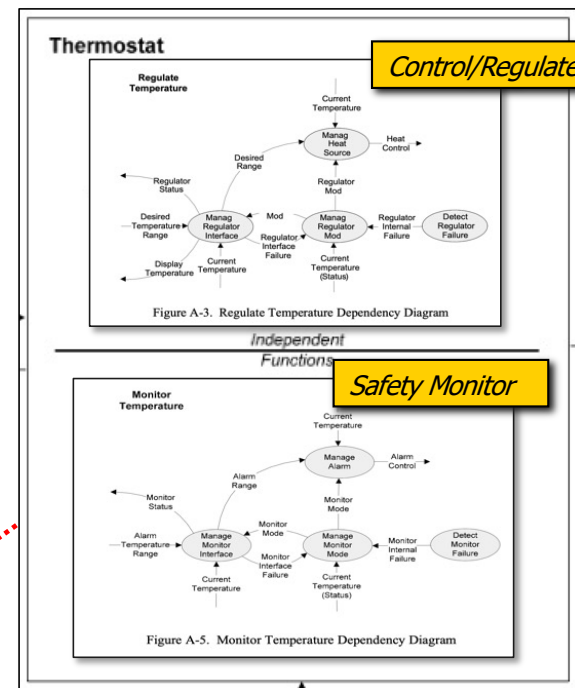
HAMR - SysMLv2/AADL to Rust + seL4

# REMH - Informal Designs

The FAA REMH decomposes the Isolette into a control system and safety monitor subsystem with three tasks each

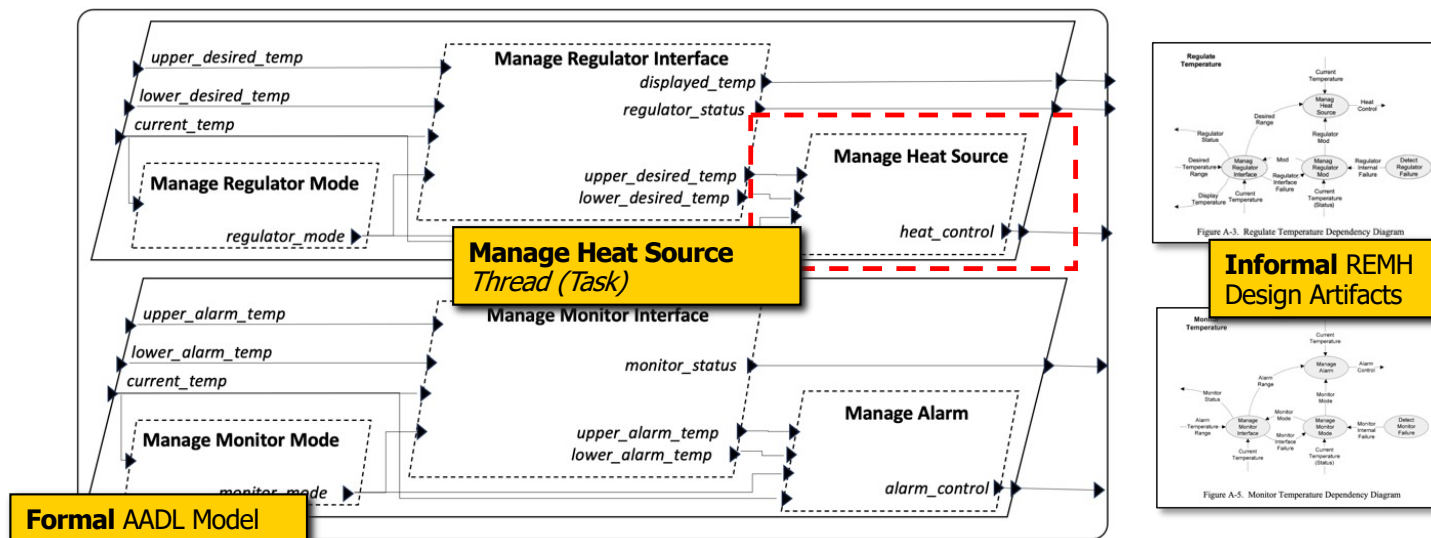


*Thermostat decomposed into Regulate Temperature and Monitor Temperature functions.*



# Using AADL to Represent Design

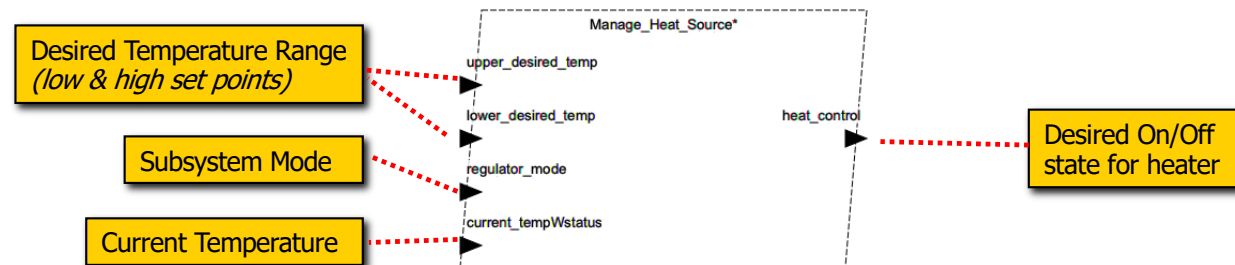
AADL Model is a straightforward rendering of the design diagrams in the FAA REMH



*This example (software aspects) is worked **completely end-to-end** from requirements, to contracts, to automatically tested and verified application code, to deployment on seL4, Linux, JVM, JavaScript. **All artifacts are publicly available.***

# Manage Heat Source Thread

## AADL Interface for **Manage Heat Source** Thread



**thread** Manage\_Heat\_Source  
**features**

-- ===== INPUTS =====

-- ("Current Temperature") - current temperature (from temp sensor)

current\_tempWstatus: **in data port** Isolette\_Data\_Model::TempWstatus.impl;

-- ("Desired Range") - lowest and upper bound of desired temperature range

lower\_desired\_temp: **in data port** Isolette\_Data\_Model::Temp.impl;

upper\_desired\_temp: **in data port** Isolette\_Data\_Model::Temp.impl;

-- ("Regulator Mode") - subsystem mode

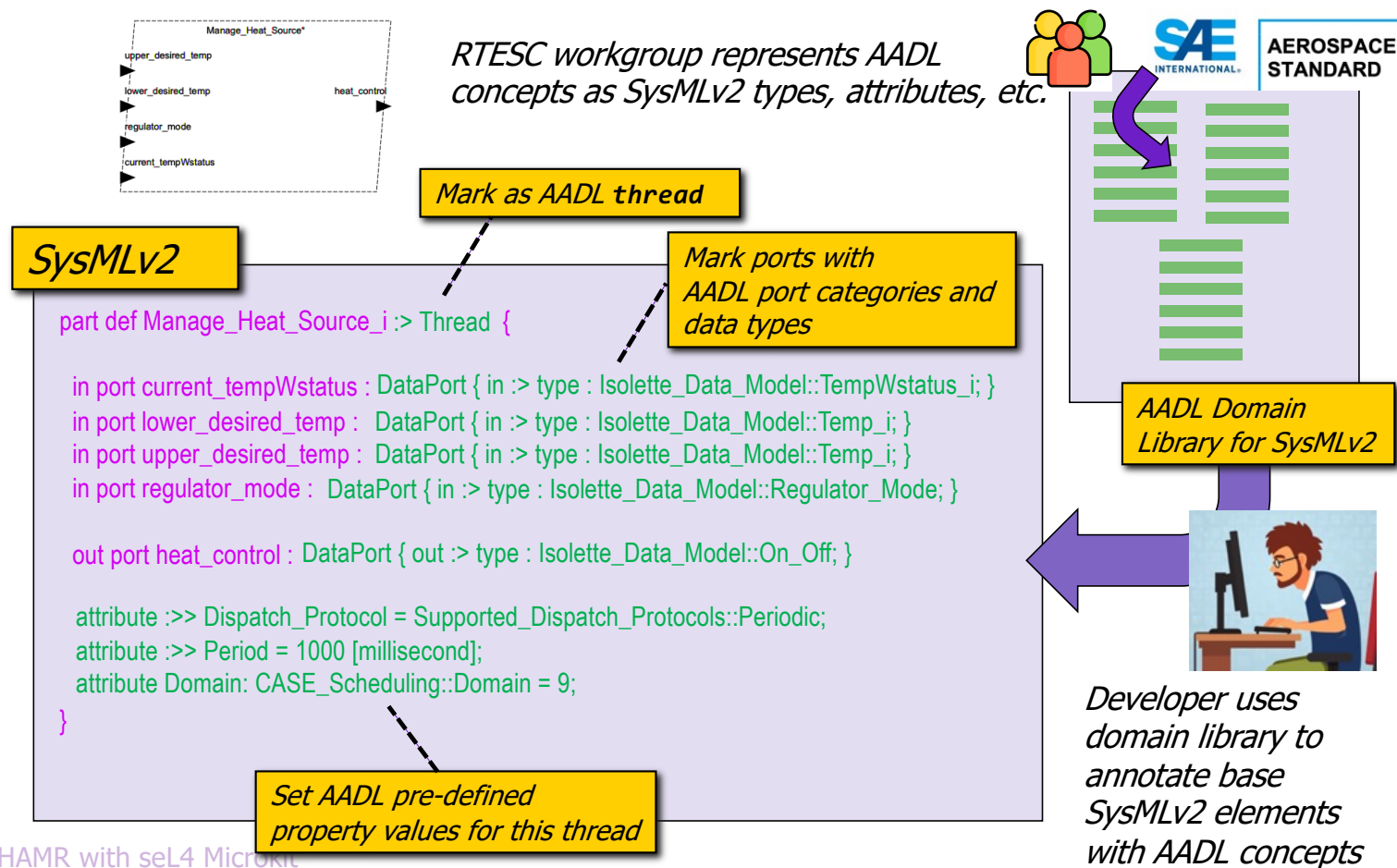
regulator\_mode: **in data port** Isolette\_Data\_Model::Regulator\_Mode;

-- ===== OUTPUTS =====

-- ("Heat Control") - command to turn heater on/off (actuation command)

heat\_control: **out data port** Isolette\_Data\_Model::On\_Off;

# SysMLv2 + AADL Modeling Concepts



# AADL / SysMLv2 Component Types Side-by-Side

## AADL

```
thread Manage_Heat_Source
features
  current_tempWstatus: in data port Isolette_Data_Model::TempWstatus.impl;
  lower_desired_temp: in data port Isolette_Data_Model::Temp.impl;
  upper_desired_temp: in data port Isolette_Data_Model::Temp.impl;
  regulator_mode: in data port Isolette_Data_Model::Regulator_Mode;
  heat_control: out data port Isolette_Data_Model::On_Off;

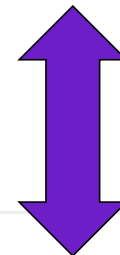
properties
  Dispatch_Protocol => Periodic;
  Period => Isolette_Properties::ThreadPeriod;
```

## SysMLv2

```
part def Manage_Heat_Source_i :> Thread {

  in port current_tempWstatus : DataPort { in :> type : Isolette_Data_Model::TempWstatus_i; }
  in port lower_desired_temp : DataPort { in :> type : Isolette_Data_Model::Temp_i; }
  in port upper_desired_temp : DataPort { in :> type : Isolette_Data_Model::Temp_i; }
  in port regulator_mode : DataPort { in :> type : Isolette_Data_Model::Regulator_Mode; }
  out port heat_control : DataPort { out :> type : Isolette_Data_Model::On_Off; }

  attribute :>> Dispatch_Protocol = Supported_Dispatch_Protocols::Periodic;
  attribute :>> Period = 1000 [millisecond];
  attribute Domain: CASE_Scheduling::Domain = 9;
```



*Appearance is similar*

# Challenges

## Challenges in migrating AADL Formal Methods to SysMLv2

- SysMLv2 has no “annex mechanism”; need to figure out how to represent AADL Annexes
  - behavior contracts, architectural constraints language, hazard analysis
- Representation of AADL Properties
  - model configuration parameters
- Formal semantics of run-time behavior
  - Development of SysMLv2 “semantics” and “formal methods” is spread across several OMG working groups and is struggling to focus
  - SysMLv2 is big and general, so it is hard for committees to develop a precise semantics that satisfies their committee mandate

# Natural Language Requirements for Thread

FAA REMH requirements for **Manage Heat Source** task

DOT/FAA/AR-08/32  
Air Traffic Organization  
Research & Operations Planning  
Office of Research and  
Technology Development  
Washington, DC 20591

Requirements Engineering  
Management Handbook

Requirements for control laws of this task...

REQ-MHS-1: If the Regulator Mode is INIT, the Heat Control shall be set to Off.

Rationale: A regulator that is initializing cannot regulate the Current Temperature of the Isolette and the Heat Control should be turned off.

REQ-MHS-2: If the Regulator Mode is NORMAL and the Current Temperature is less than the Lower Desired Temperature, the Heat Control shall be set to On.

REQ-MHS-3: If the Regulator Mode is NORMAL and the Current Temperature is greater than the Upper Desired Temperature, the Heat Control shall be set to Off.

REQ-MHS-4: If the Regulator Mode is NORMAL and the Current Temperature is greater than or equal to the Lower Desired Temperature and less than or equal to the Upper Desired Temperature, the value of the Heat Control shall not be changed.

REQ-MHS-5: If the Regulator Mode is FAILED, the Heat Control shall be set to Off.

Available to the U.S. public through  
Information Service (NTIS),  
2161.

Reportation  
Illustration

# Component Requirements to Contracts

GUMBO contracts are written together with the thread interface in the VSCode SysIDE plug-in **using a customized editor extension that we developed to support contracts**

The screenshot displays the VSCode SysIDE interface with the SysML file 'Regulate.sysml' open. The code defines a component 'Manage\_Heat\_Source\_1' with inputs for temperature and desired temperature, and an output for heat control. A red dashed box highlights the 'Component interface' section, which includes the input and output ports. Another red dashed box highlights the 'Component contract' section, which includes the 'GUMBO' language block and the 'REQ\_MHS\_1' requirement. A yellow box on the right lists 'Heat Controller Task natural language functional requirements (control laws)' with five requirements (REQ-MHS-1 to REQ-MHS-5). A yellow box on the left states 'Contracts incorporated via SysMLv2 language construct (essentially, a comment that HAMR parses, highlights syntax, etc.)'. A yellow box at the bottom right says 'Developer formalizes requirements'. A small image of a baby in a hospital bed is visible in the bottom right corner.

**Component interface**

**Component contract**

**Heat Controller Task natural language functional requirements (control laws)**

**Contracts incorporated via SysMLv2 language construct (essentially, a comment that HAMR parses, highlights syntax, etc.)**

**Developer formalizes requirements**

HAMR - SysMLv2/AADL to Rust + seL4

# Component Requirements to Contracts

**Example:** One contract from *heater control laws* in **Manage Heat Source** Thread (a periodic component), with traceability to natural language requirements.

Mode condition  
(*..if the mode is Normal*)

...

Compare current temperature to desired range  
(*..if temperature is below the target range*)

```
case REQ_MHS_2 "If the Regulator Mode is NORMAL and the Current Temperature is less than  
|the Lower Desired Temperature, the Heat Control shall be set to On.":  
  assume (regulator_mode == Isolette_Data_Model::Regulator_Mode.Normal_Regulator_Mode)  
    & (current_tempWstatus.value < lower_desired_temp.value);  
  guarantee heat_control == Isolette_Data_Model::On_Off.Onn;  
...
```

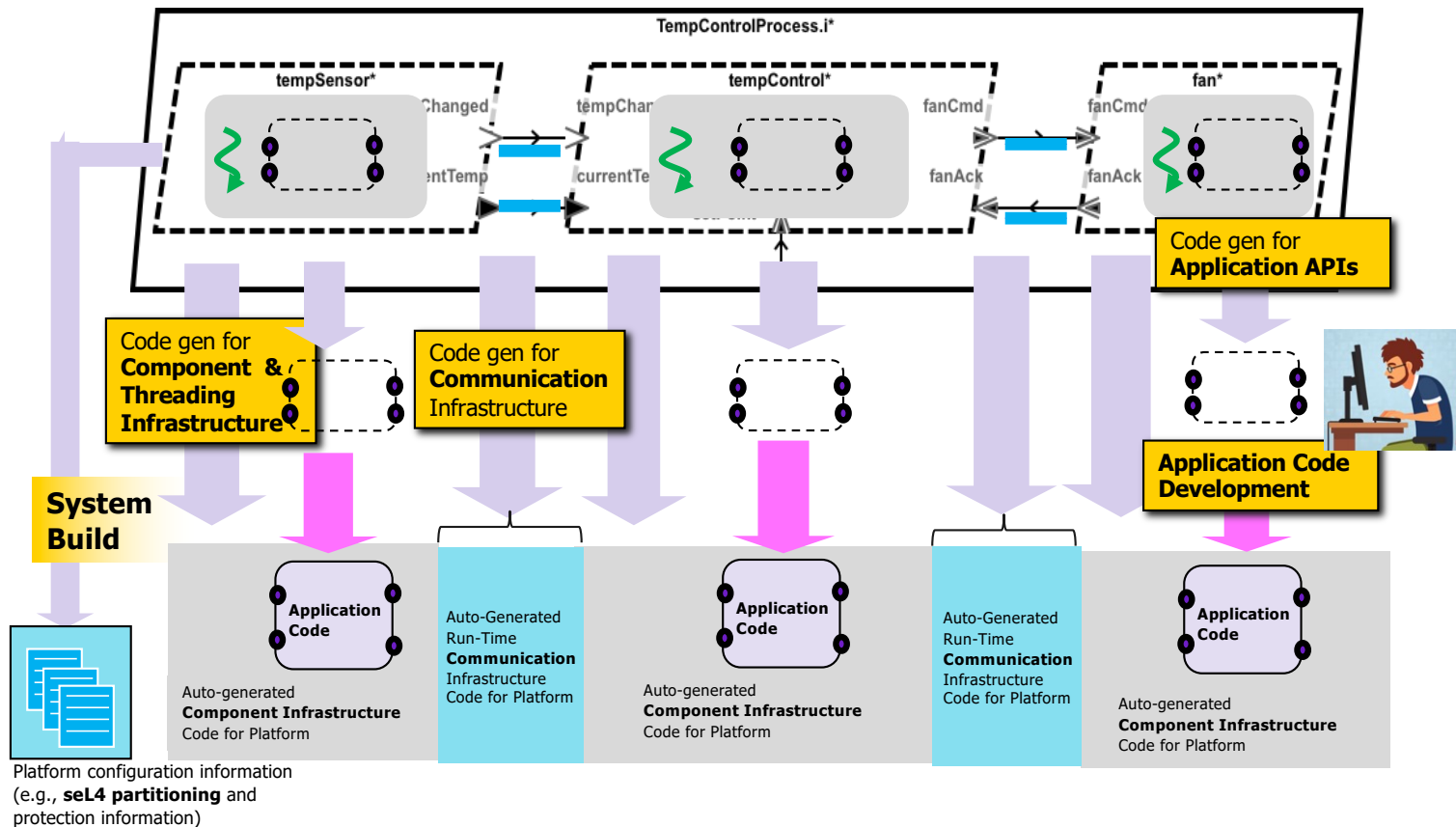
...

Set the desired state of the heater  
(*...turn heater On, to warm up the Isolette*)



OSATE AADL Editor

# HAMR Code Generation

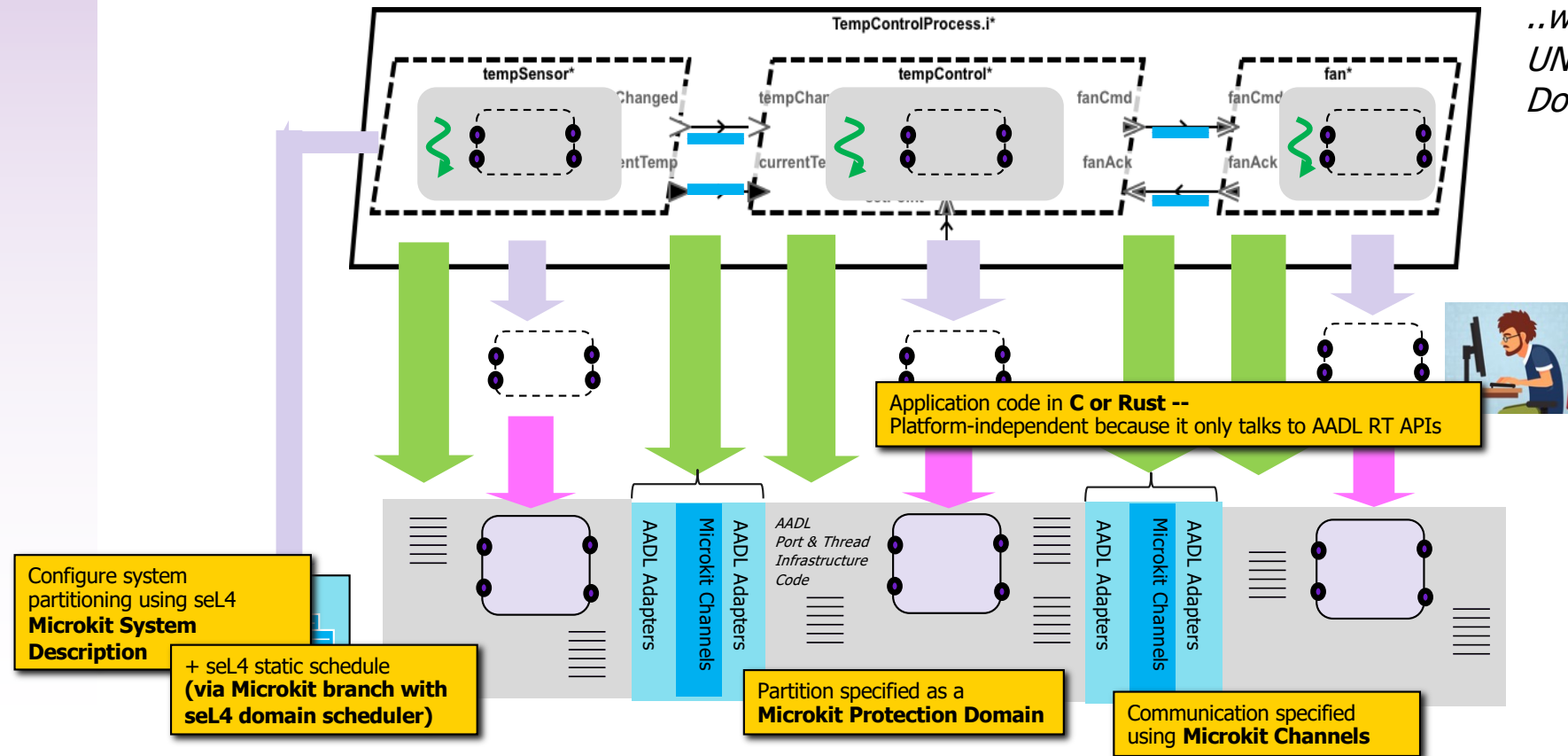


HAMR - SysMLv2/AADL to Rust + seL4

# HAMR Code Generation

For seL4, the process is instantiated like this...

*..working with  
UNSW and  
DornerWorks*



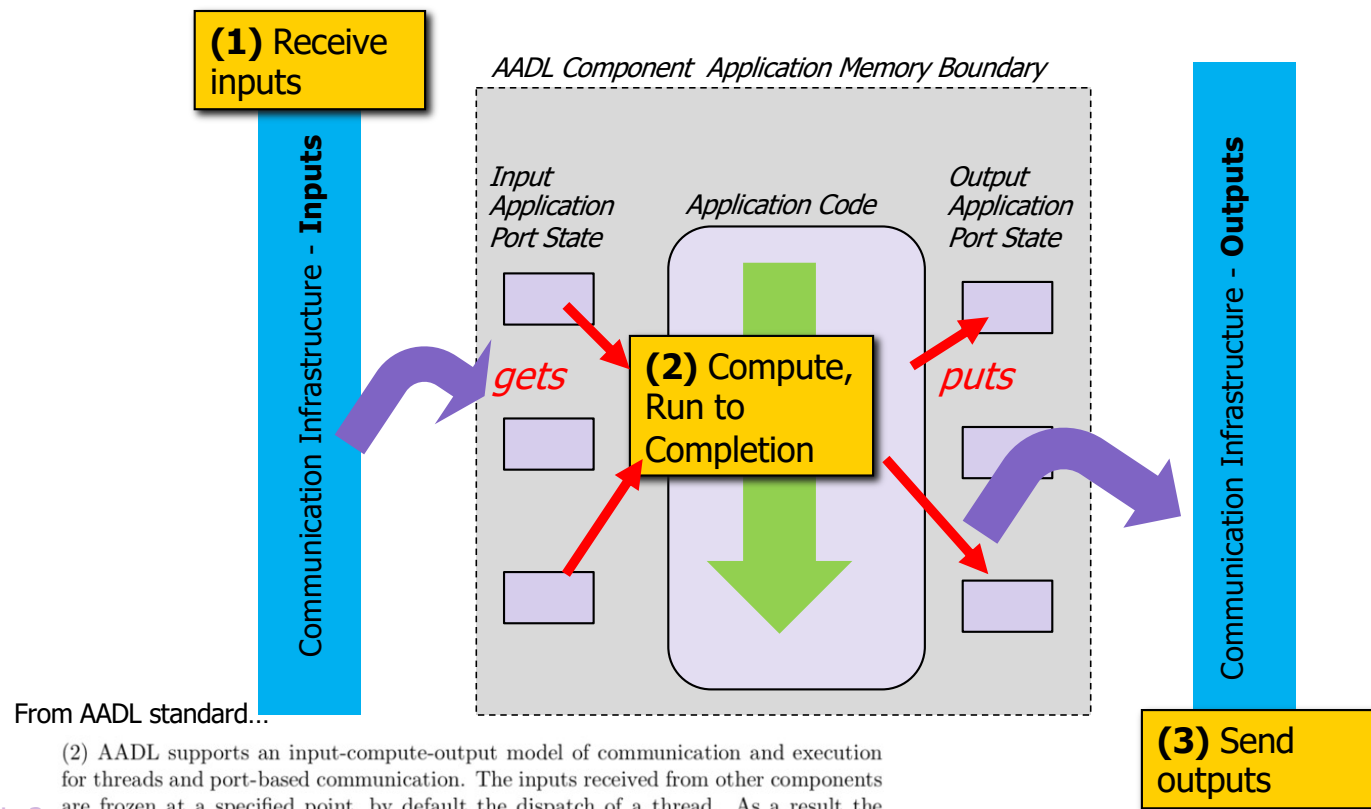
SysMLv2/AADL for HAMR with seL4 Microkit

# AADL Port and Thread Execution Semantics



"Analyzeable Real-Time Systems"  
Burns & Wellings

On each dispatch, AADL threads follow a well-known **input-compute-output** pattern for real-time tasks that simplifies analysis and verification...

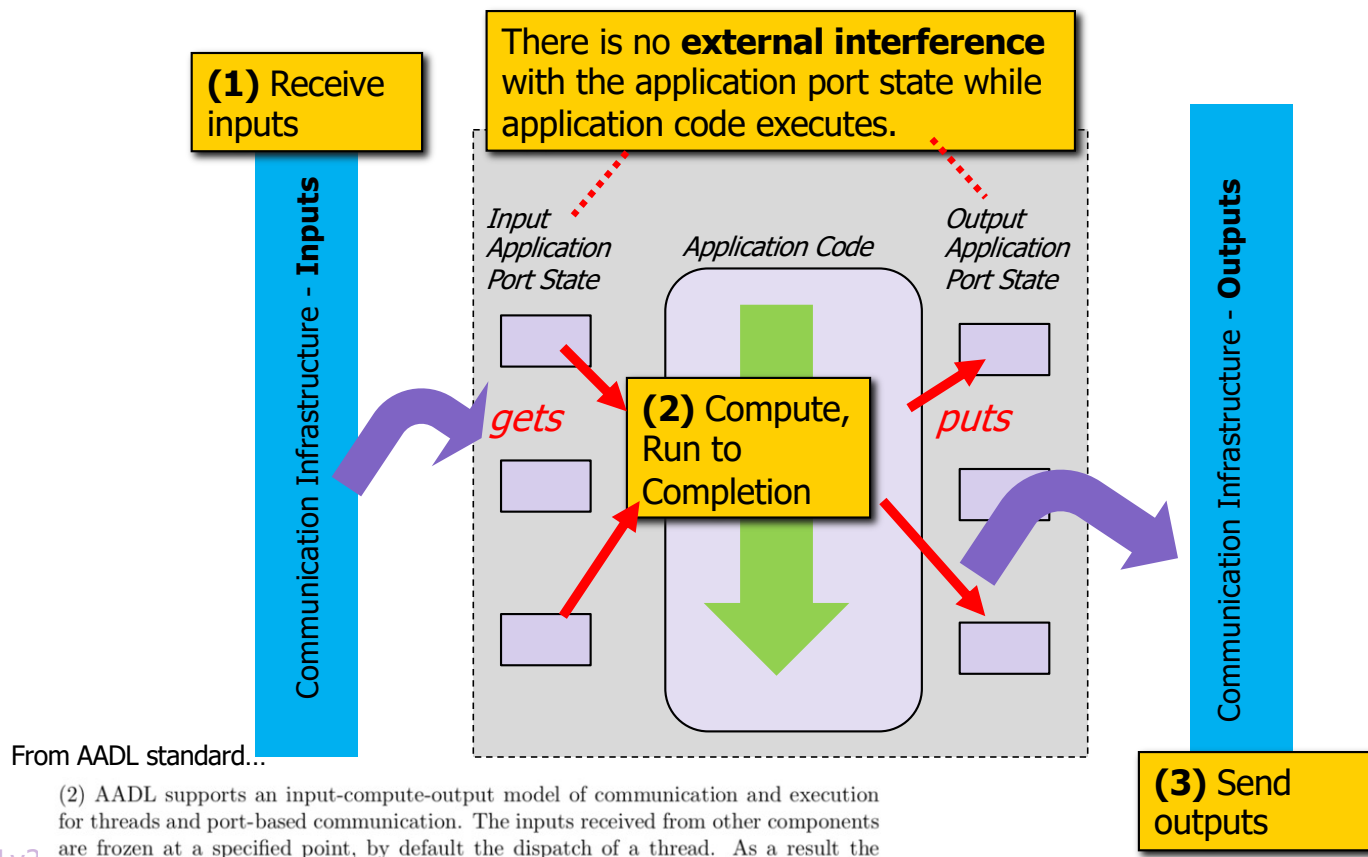


# AADL Port and Thread Execution Semantics



"Analyzeable Real-Time Systems"  
Burns & Wellings

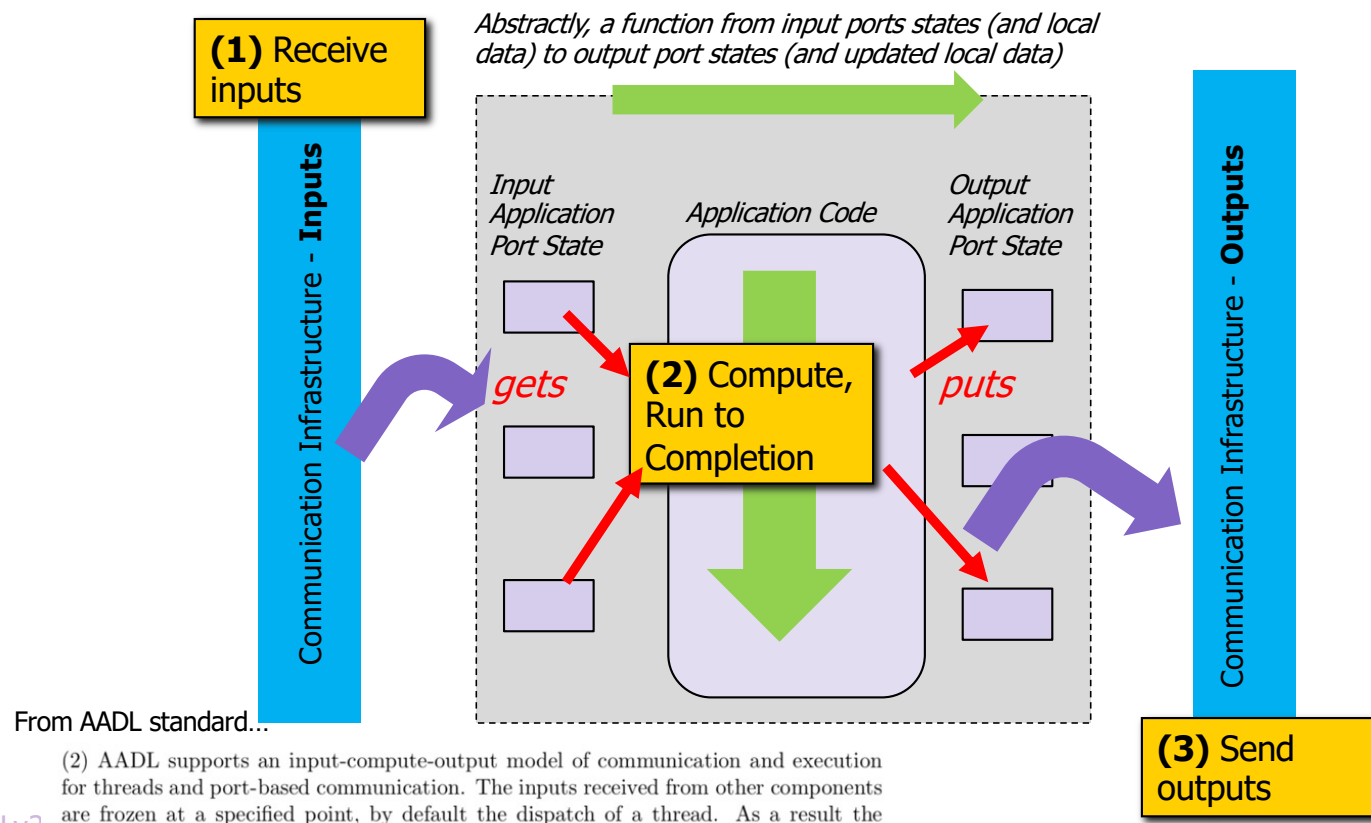
AADL tasking and port semantics ensures no interference with other threads or communication layer



# AADL Port and Thread Execution Semantics



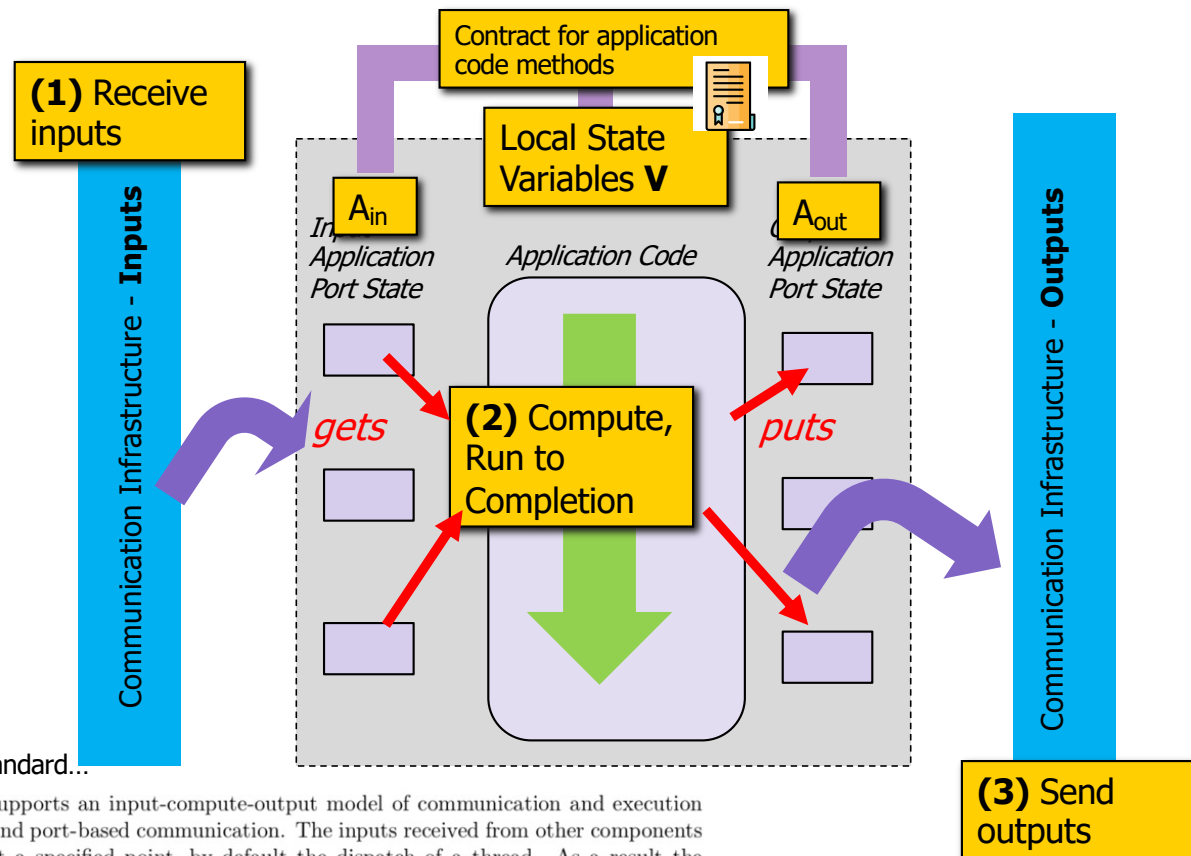
"Analyzeable Real-Time Systems"  
Burns & Wellings



# AADL Port and Thread Execution Semantics



"Analyzeable Real-Time Systems"  
Burns & Wellings

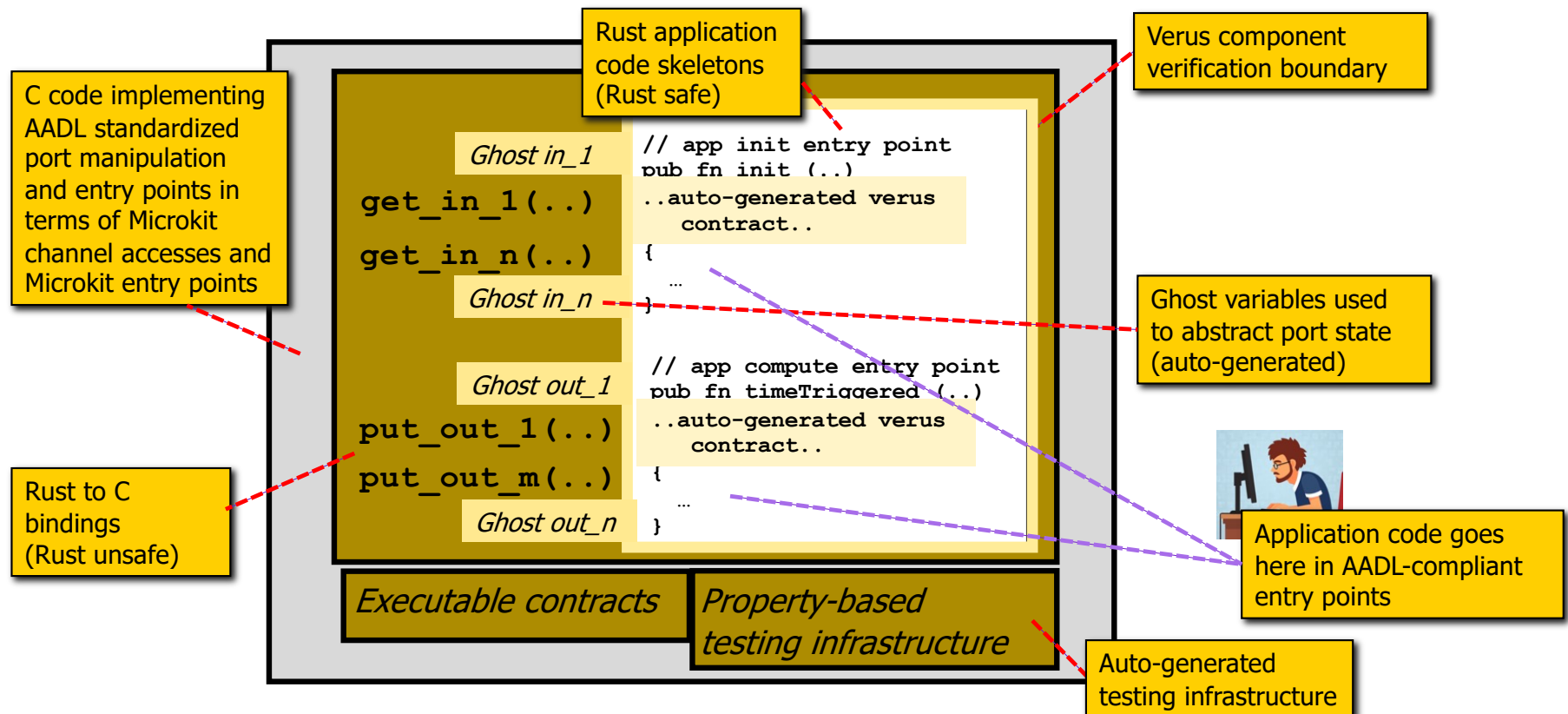


From AADL standard...

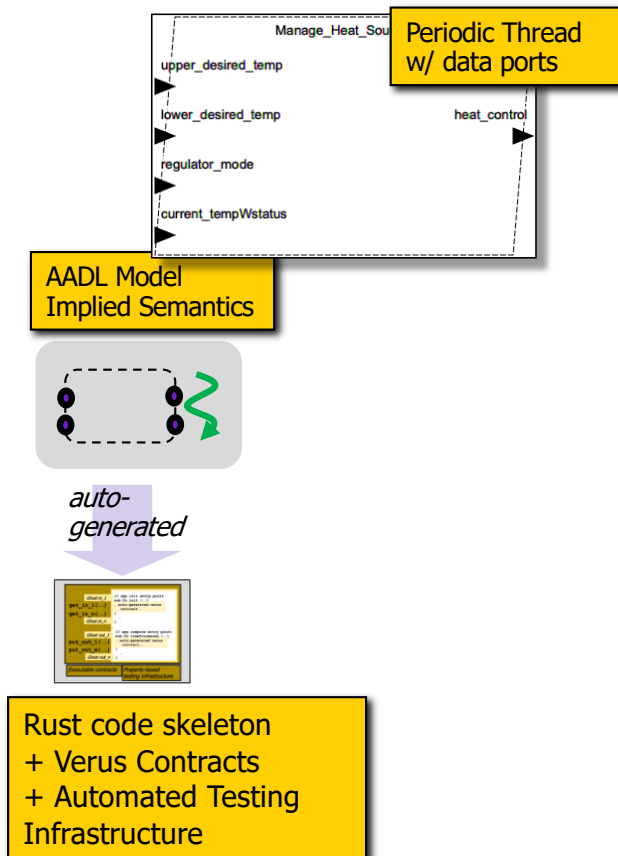
(2) AADL supports an input-compute-output model of communication and execution for threads and port-based communication. The inputs received from other components are frozen at a specified point, by default the dispatch of a thread. As a result the

# Outline of Protection Domain Structure

For each SysMLv2/AADL *periodic Thread* component, HAMR generates the following Microkit PD code...



# Auto-generated Skeleton, Contracts, Testing



.....*Interfaces/APIs/Skeletons + **contracts** + **testing infrastructure*** are auto-generated from SysMLv2/AADL model.

# Auto-generated Skeleton, Contracts, Testing

.....Interfaces/APIs/Skeletons + **contracts** + **testing infrastructure** are auto-generated from SysMLv2/AADL model.

**Periodic Thread w/ data ports**

**AADL Model Implied Semantics**

**auto-generated**

**Application Code in Rust**

**Rust VSCode editor**

**Component contract (small excerpt)**

```
pub fn timeTriggered() {
    (old(api).regulator_mode == Isolette_Data_Model::Regulator_Mode::Failed_Regulator_Mode)
    (api.heat_control == Isolette_Data_Model::On_Off::Off)
    // END MARKER TIME TRIGGERED ENSURES
}
```

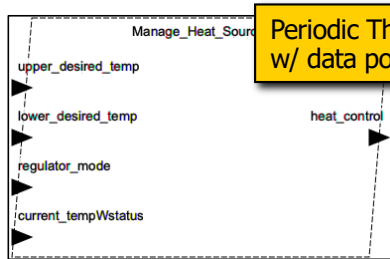
**Skeleton for application code entry point**

**postcondition not satisfied**

Verus error indicates that contract is not yet satisfied

HAMK - SysMLv2/AADL to Rust + sel4

# Verus Contract Auto-Generated From Model Contract



Periodic Thread  
w/ data ports

auto-  
generated



Verification of Rust application code against contracts using Verus (excerpts)

```
57 pub fn timeTriggered<API: thermostat_rt_mhs_mhs_Full_Api>(  
58     &mut self,  
59     api: &mut thermostat_rt_mhs_mhs_Application_Api<API>)  
60     requires  
61         // BEGIN MARKER TIME TRIGGERED REQUIRES  
62         // assume lower_is_lower_temp  
63         old(api).lower_desired_temp.degrees <= old(api).upper_desired_temp.degrees  
64         // END MARKER TIME TRIGGERED REQUIRES  
65     ensures  
66         // BEGIN MARKER TIME TRIGGERED ENSURES  
67         // guarantee lastCmd
```

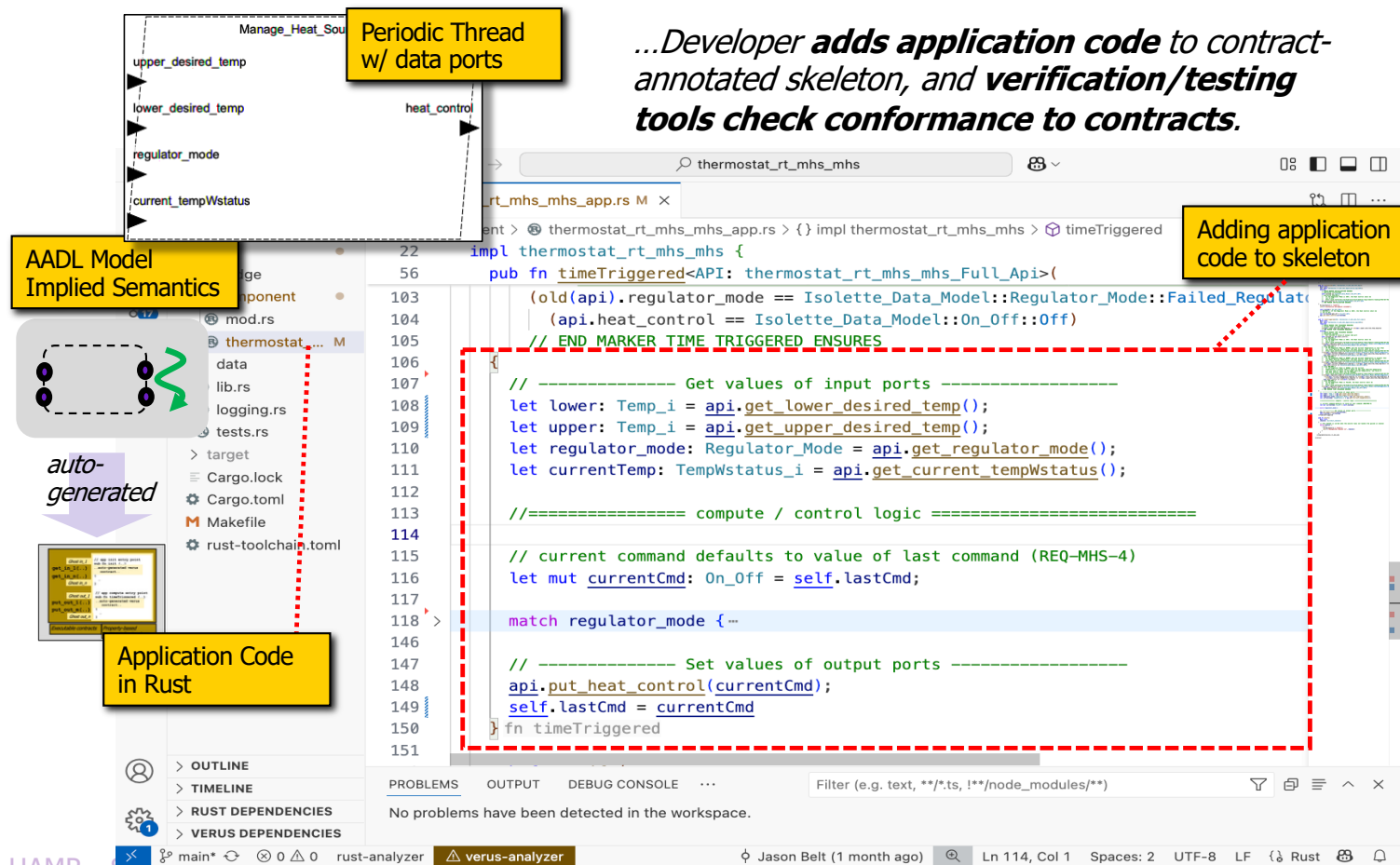
Pre

Post

```
// case REQ_MHS_2  
// If the Regulator Mode is NORMAL and the Current Temperature is less than  
// the Lower Desired Temperature, the Heat Control shall be set to On.  
((old(api).regulator_mode == Regulator_Mode::Normal_Regulator_Mode) &&  
 (old(api).current_tempWstatus.degrees < old(api).lower_desired_temp.degrees)) ==>  
 (api.heat_control == On_Off::Onn),
```

```
76 // If the Regulator Mode is NORMAL and the Current Temperature is less than  
77 // the Lower Desired Temperature, the Heat Control shall be set to On.  
78 ((old(api).regulator_mode == Regulator_Mode::Normal_Regulator_Mode) &&  
79 (old(api).current_tempWstatus.degrees < old(api).lower_desired_temp.degrees)) ==>  
80 (api.heat_control == On_Off::Onn),
```

# Coding and Background Verification



# Coding and Background Verification

...Developer uses auto-generate APIs to **get** and **put** data on component ports

Periodic Thread w/ data ports

Get

Put

Reading a value from the `regulator_mode` input data port using auto-generated API

Putting a value from the `heat_control` output data port using auto-generated API

AADL Model Implied Semantics

auto-generated

Application Code in Rust

Verus indicates that contract is satisfied

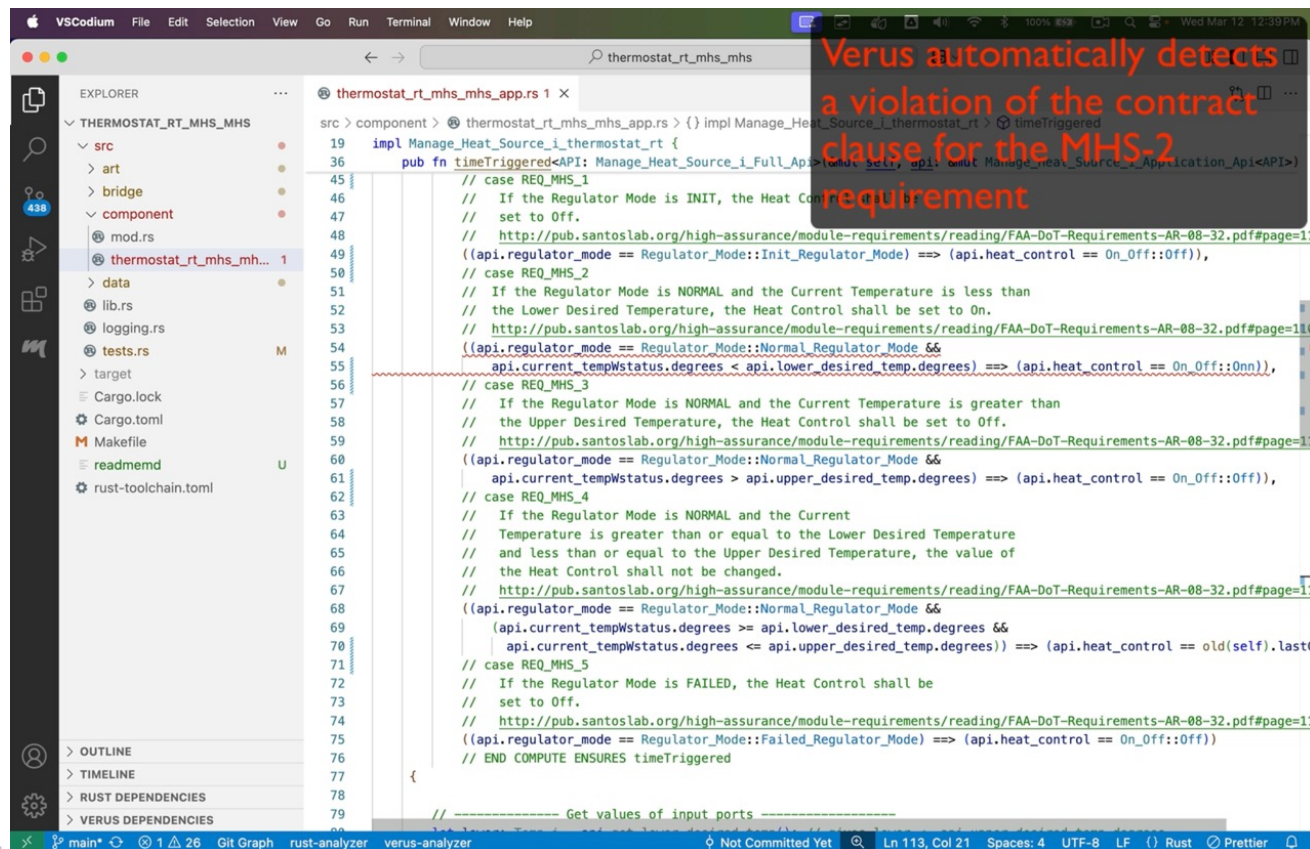
No problems have been detected in the workspace.

```
22  impl thermostat_rt_mhs_mhs {
56  pub fn timeTriggered<API: thermostat_rt_mhs_mhs_Full_Api>(<
103    (old(api).regulator_mode == Isolette_Data_Model::Regulator_Mode::Failed_Regulator
104    (api.heat_control == Isolette_Data_Model::On_Off::Off)
105    // END MARKER TIME TRIGGERED ENSURES
106
107    // ----- Get values of input ports -----
108    let lower: Temp_i = api.get_lower_desired_temp();
109    let upper: Temp_i = api.get_upper_desired_temp();
110    let regulator_mode: Regulator_Mode = api.get_regulator_mode();
111    let currentTemp: TempWstatus_i = api.get_current_tempwstatus();
112
113    //===== compute / control logic =====
114
115    // current command defaults to value of last command (REQ-MHS-4)
116    let mut currentCmd: On_Off = self.lastCmd;
117
118    match regulator_mode {
146
147    // ----- Set values of output ports -----
148    api.put_heat_control(currentCmd);
149    self.lastCmd = currentCmd;
150  }
151  fn timeTriggered
```

HAMK - SysMLV2/AADL to Rust + Self

# Demo

Verification of application code against contracts using Verus verification tool...



The screenshot shows the VSCode editor with a Rust project named 'thermostat\_rt\_mhs\_mhs'. The Explorer panel on the left shows the project structure, including 'src', 'component', 'mod.rs', 'data', 'lib.rs', 'logging.rs', 'tests.rs', 'target', 'Cargo.lock', 'Cargo.toml', 'Makefile', 'readmemd', and 'rust-toolchain.toml'. The main editor displays the file 'thermostat\_rt\_mhs\_mhs\_app.rs' with the following code:

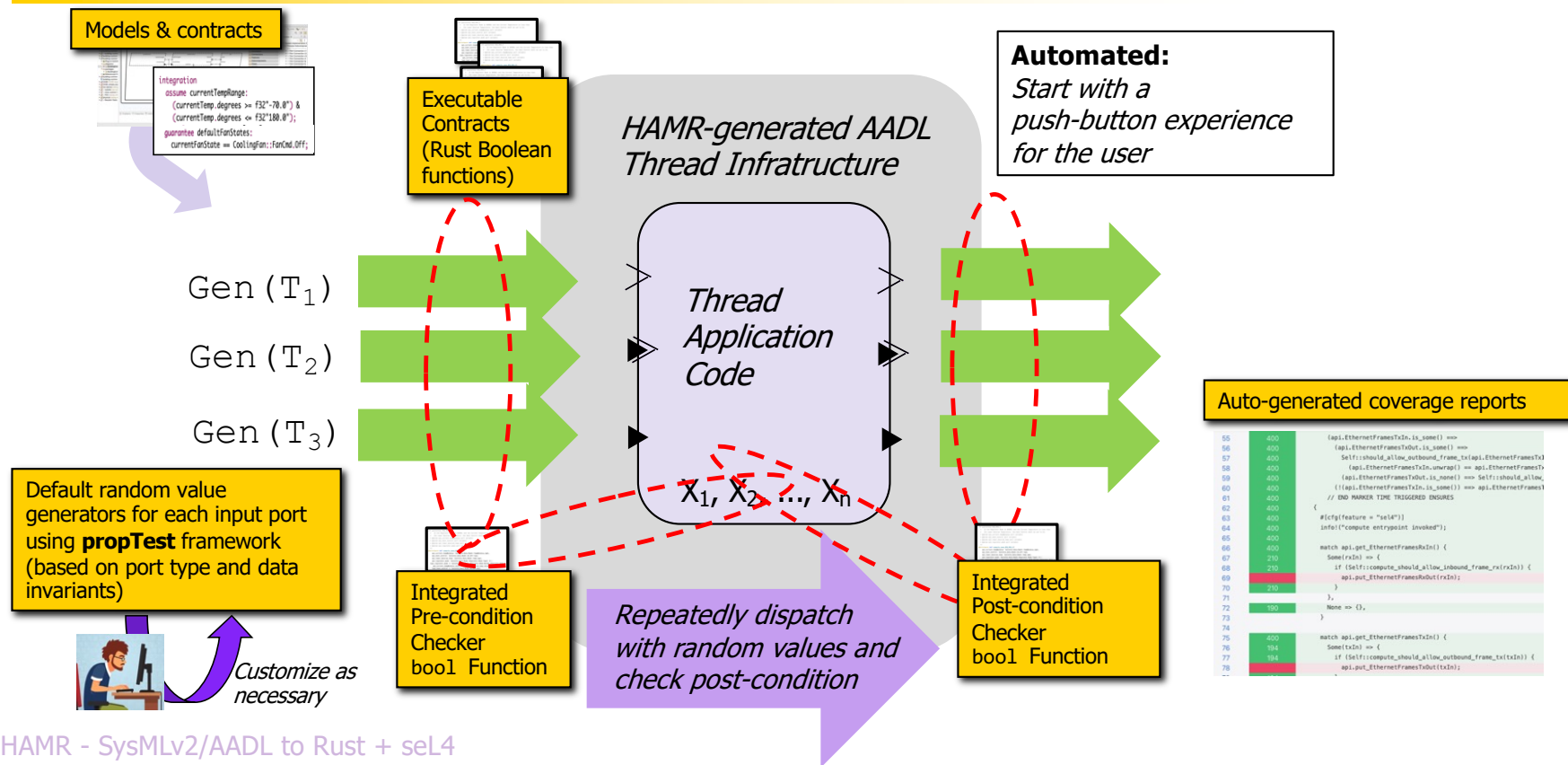
```
src > component > thermostat_rt_mhs_mhs_app.rs > {} impl Manage_Heat_Source_i_thermostat_rt {
19 impl Manage_Heat_Source_i_thermostat_rt {
36 pub fn timeTriggered<API: Manage_Heat_Source_i_Full_Api>(mut self, api: &mut Manage_Heat_Source_i_Application_Api<API>) {
45 // case REQ_MHS_1
46 // If the Regulator Mode is INIT, the Heat Control shall be set to Off.
47 // set to Off.
48 // http://pub.santoslab.org/high-assurance/module-requirements/reading/FAA-DoT-Requirements-AR-08-32.pdf#page=11
49 ((api.regulator_mode == Regulator_Mode::Init_Regulator_Mode) ==> (api.heat_control == On_Off::Off)),
50 // case REQ_MHS_2
51 // If the Regulator Mode is NORMAL and the Current Temperature is less than
52 // the Lower Desired Temperature, the Heat Control shall be set to On.
53 // http://pub.santoslab.org/high-assurance/module-requirements/reading/FAA-DoT-Requirements-AR-08-32.pdf#page=11
54 ((api.regulator_mode == Regulator_Mode::Normal_Regulator_Mode &&
55 api.current_tempWstatus.degrees < api.lower_desired_temp.degrees) ==> (api.heat_control == On_Off::On)),
56 // case REQ_MHS_3
57 // If the Regulator Mode is NORMAL and the Current Temperature is greater than
58 // the Upper Desired Temperature, the Heat Control shall be set to Off.
59 // http://pub.santoslab.org/high-assurance/module-requirements/reading/FAA-DoT-Requirements-AR-08-32.pdf#page=11
60 ((api.regulator_mode == Regulator_Mode::Normal_Regulator_Mode &&
61 api.current_tempWstatus.degrees > api.upper_desired_temp.degrees) ==> (api.heat_control == On_Off::Off)),
62 // case REQ_MHS_4
63 // If the Regulator Mode is NORMAL and the Current
64 // Temperature is greater than or equal to the Lower Desired Temperature
65 // and less than or equal to the Upper Desired Temperature, the value of
66 // the Heat Control shall not be changed.
67 // http://pub.santoslab.org/high-assurance/module-requirements/reading/FAA-DoT-Requirements-AR-08-32.pdf#page=11
68 ((api.regulator_mode == Regulator_Mode::Normal_Regulator_Mode &&
69 (api.current_tempWstatus.degrees >= api.lower_desired_temp.degrees &&
70 api.current_tempWstatus.degrees <= api.upper_desired_temp.degrees)) ==> (api.heat_control == old(self).lastC
71 // case REQ_MHS_5
72 // If the Regulator Mode is FAILED, the Heat Control shall be
73 // set to Off.
74 // http://pub.santoslab.org/high-assurance/module-requirements/reading/FAA-DoT-Requirements-AR-08-32.pdf#page=11
75 ((api.regulator_mode == Regulator_Mode::Failed_Regulator_Mode) ==> (api.heat_control == On_Off::Off))
76 // END COMPUTE ENSURES timeTriggered
77 {
78 // ----- Get values of input ports -----
79 }
```

Overlaid on the code is a red text box with the message: "Verus automatically detects a violation of the contract clause for the MHS-2 requirement".

HAMK - SysMLV2/AADL to Rust + sel4

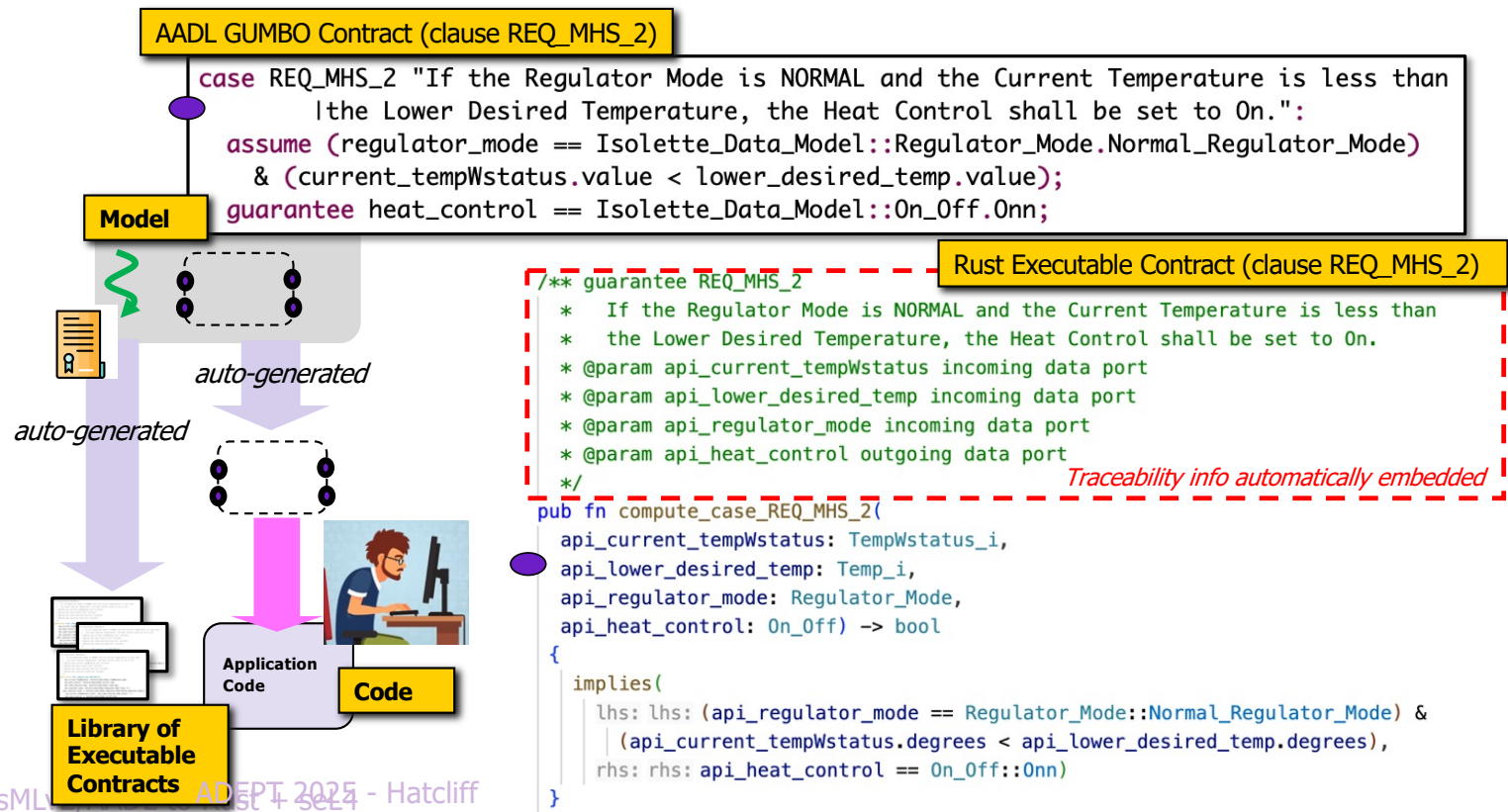
# Automated Testing to Contracts

For every thread component, HAMR auto-generates property-based testing infrastructure for inserting values into component input ports and for checking values of output ports.



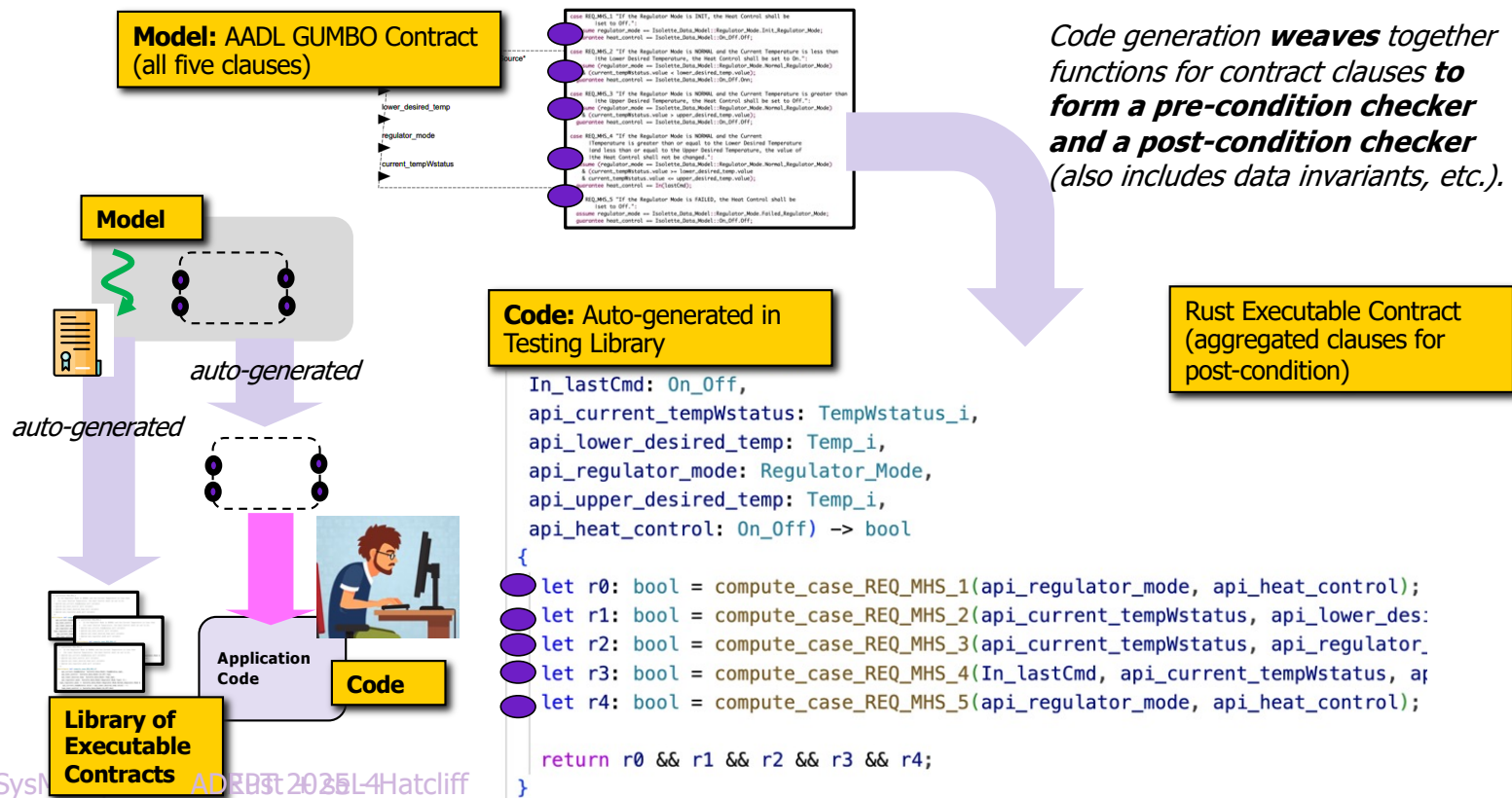
# HAMR-generated *Executable* Contracts

Each clause in **model-level** GUMBO contracts is translated to a **code-level** Boolean function in Rust that works on the appropriate port/thread state elements



# HAMR-generated *Executable* Contracts

Complete set of **Model-level** GUMBO contract clauses are translated to a hierarchy of executable Boolean functions in Rust (**code-level**) to form executable pre/post conditions and test oracles.



# HAMR-generated Randomizing Test Runner

HAMR automatically generates test runner infrastructure with default random value generators for each input port. The executable contract is automatically used behind the scenes as a test oracle.

```
testComputeCB_macro! {
```

```
  ▶ Run Test | Debug
```

```
  prop_testComputeCB_default, // test name
```

```
  config: ProptestConfig { // proptest configuration, built by overriding fields from default config
```

```
    cases: numValidComputeTestCases,
```

```
    max_global_rejects: numValidComputeTestCases * computeRejectRatio,
```

```
    verbose: verbosity,
```

```
    ..ProptestConfig::default()
```

```
  },
```

```
  // auto-generated strategies for generating each component input
```

```
  api_current_tempWstatus: test_api::Isolette_Data_Model_TempWstatus_i_strategy_default(),
```

```
  api_lower_desired_temp: test_api::Isolette_Data_Model_Temp_i_strategy_default(),
```

```
  api_regulator_mode: test_api::Isolette_Data_Model_Regulator_Mode_strategy_default(),
```

```
  api_upper_desired_temp: test_api::Isolette_Data_Model_Temp_i_strategy_default()
```

```
}
```

Press this button and you automatically get 1000's of random tests against the component contract



auto-generated configurations for proptest framework

auto-generated proptest random value generators for each input port

# HAMR-generated Randomizing Test Runner

Default random generators are often easy to customize to increase coverage, reduce #'s of discarded tests, obtain tests for specific features, etc.

```
testComputeCB_macro! {  
  ▶ Run Test | Debug  
  prop_testComputeCB_default, // test name  
  config: ProptestConfig { // proptest configuration, built by overriding fields from default config  
    cases: numValidComputeTestCases,  
    max_global_rejects: numValidComputeTestCases * computeRejectRatio,  
    verbose: verbosity,  
    ..ProptestConfig::default()  
  },  
}
```

Customizing a numeric generator to a particular range

```
// developer-customized strategies for generating each component input  
api_current_tempWstatus: test_api::Isolette_Data_Model_TempWstatus_i_strategy_cust(  
  95..=103,  
  test_api::Isolette_Data_Model_ValueStatus_strategy_default()),  
api_lower_desired_temp: test_api::Isolette_Data_Model_Temp_i_strategy_cust(94..=105),  
api_regulator_mode: test_api::Isolette_Data_Model_Regulator_Mode_strategy_default(),  
api_upper_desired_temp: test_api::Isolette_Data_Model_Temp_i_strategy_cust(94..=105)
```

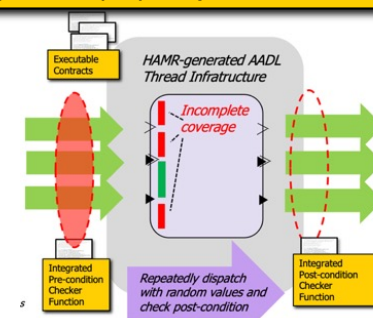


Developer-customized generators

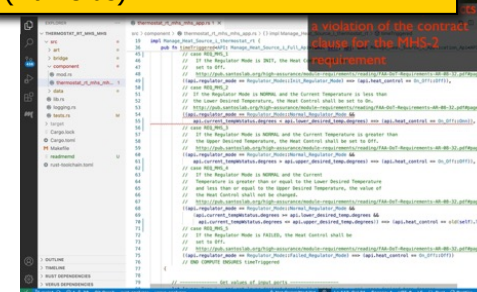
# Benefits - Integrated Testing / Verification

- Immediately launch 1000's of default tests, check conformance to contracts
  - Debug contracts; gradually move to Verus
- When Verus verification fails, generate concrete failing tests that can be given to developers to run through debugger
- When Verus/SMT cannot handle certain language features; use testing for lower-confidence assurance
  - Maybe be a step taken before handing off certain VCs from Verus to Lean
- Testing and verification *derived from the exact same GUMBO contracts*

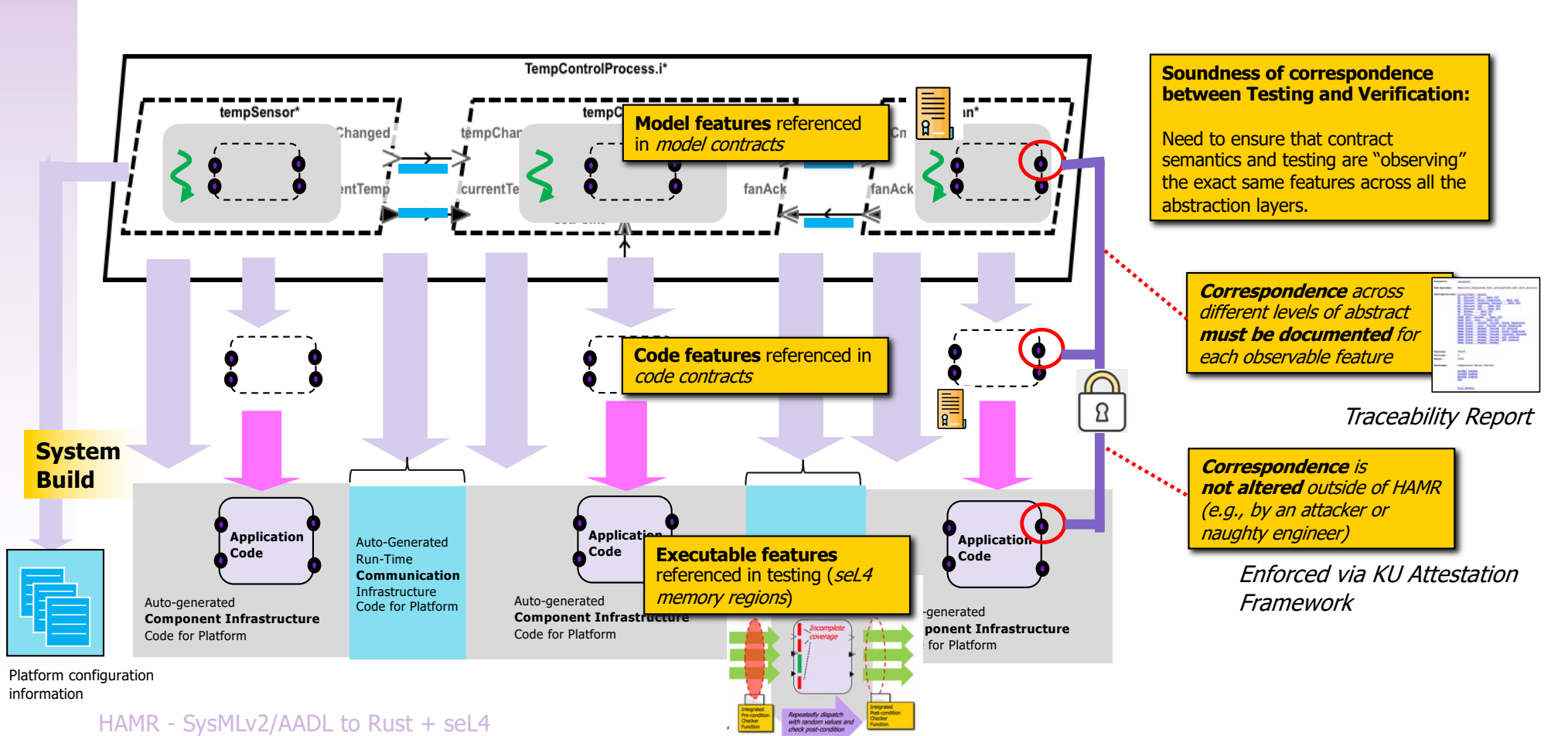
## HAMR automated component testing (via Rust propTest)



## HAMR automated verification (via Verus)

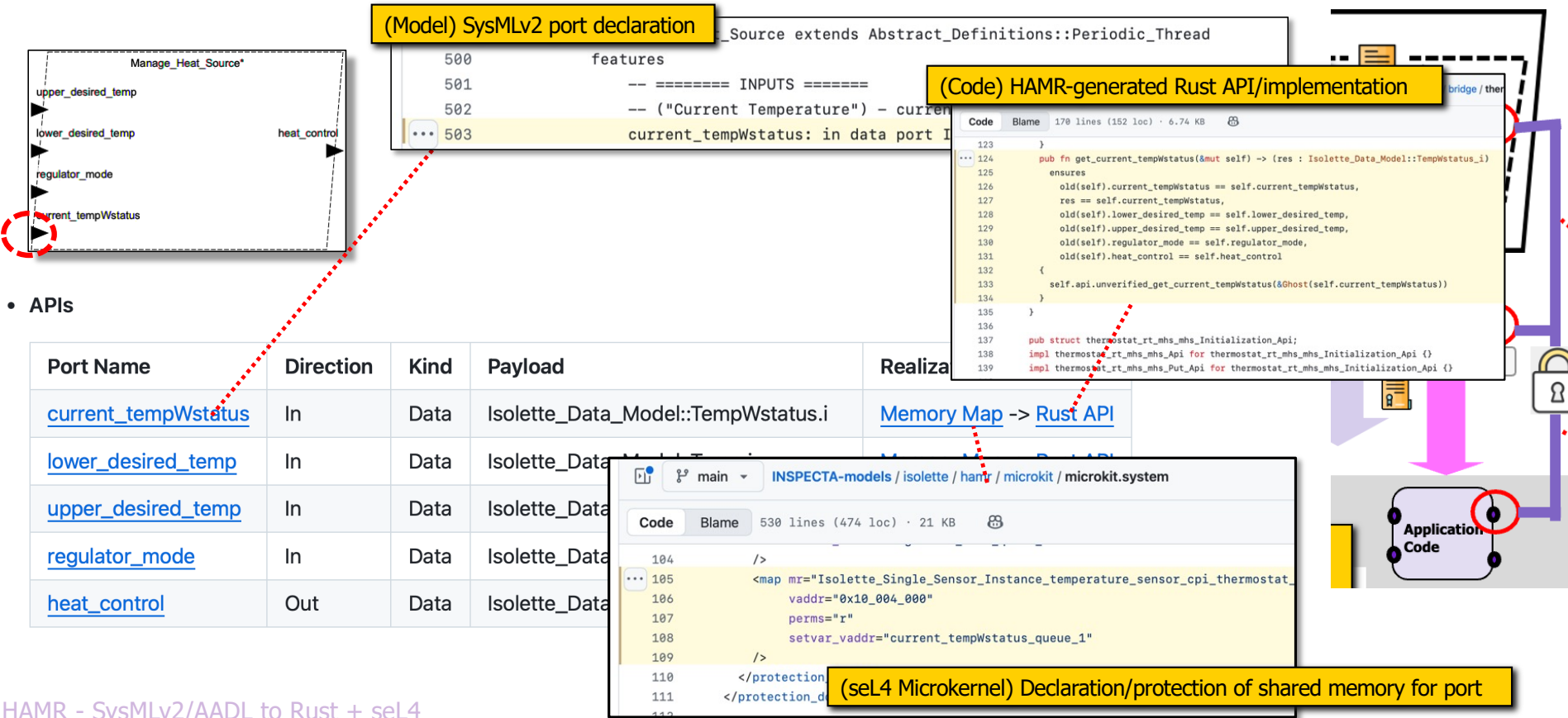


# HAMR Observations/Traceability Framework



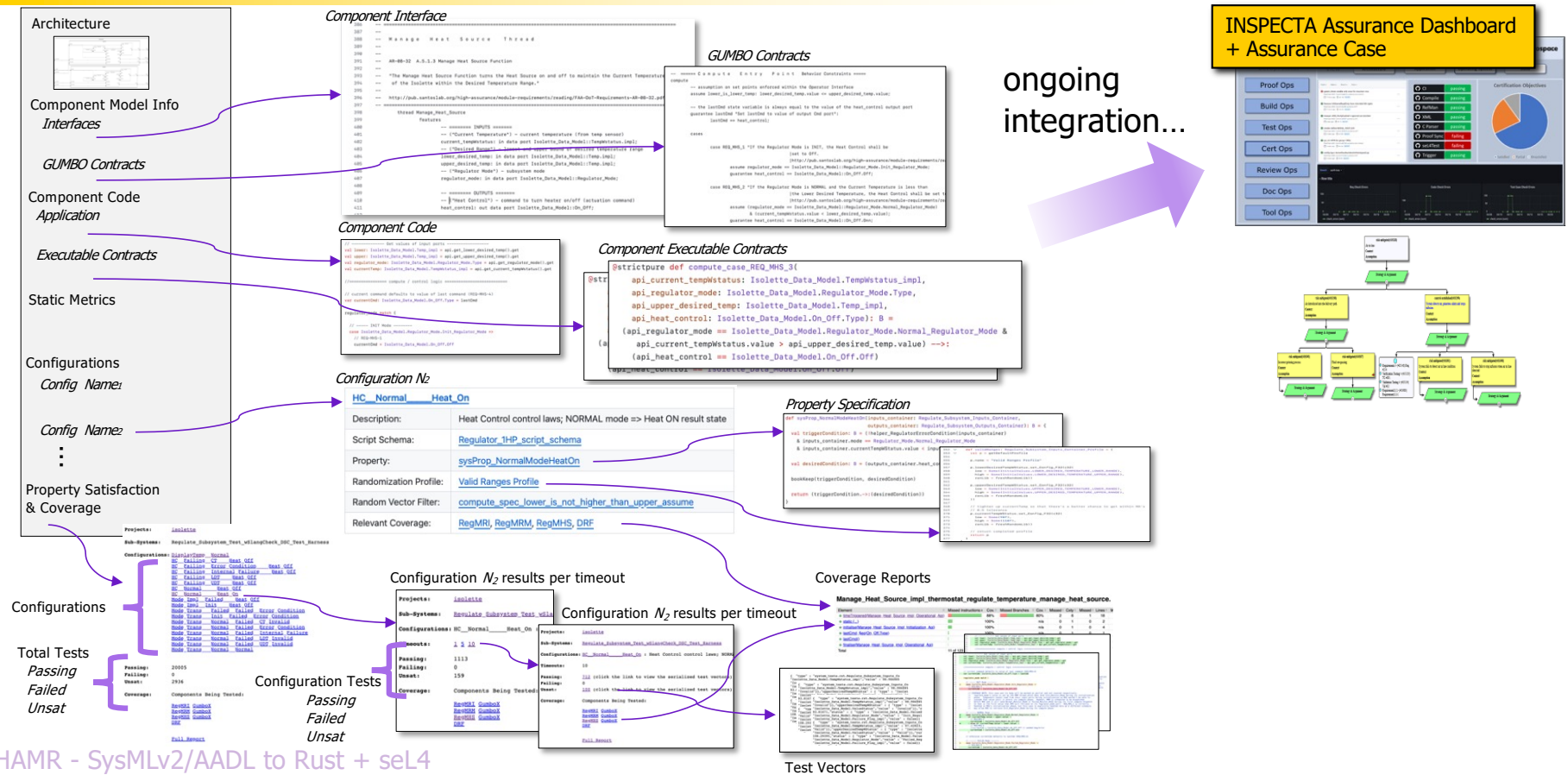
# Auto-generated System Feature Traceability for Manage Heat Source Port (GitHub Markdown)

HAMR auto-generates traceability reports, e.g., for a port – relationships between **model**, **code**, **kernel** artifacts



# Assurance and Traceability Reports

HAMR auto-generates a variety of assurance and traceability reports



HAMR - SysMLv2/AADL to Rust + seL4

# Auto-generated Contract Traceability for Manage Heat Source Requirement (GitHub Markdown)

## Contract Clause traceability

### GUMBO

#### State Variables

lastCmd

[GUMBO](#)

[Verus](#)

#### Initialize

guarantee initlastCmd

[GUMBO](#)

[Verus](#)

[GUMBOX](#)

guarantee REQ\_MHS\_1

[GUMBO](#)

[Verus](#)

[GUMBOX](#)

#### Compute

assume lower\_is\_lower\_temp

[GUMBO](#)

[Verus](#)

[GUMBOX](#)

guarantee lastCmd

[GUMBO](#)

[Verus](#)

[GUMBOX](#)

case REQ\_MHS\_1

[GUMBO](#)

[Verus](#)

[GUMBOX](#)

case REQ\_MHS\_2

[GUMBO](#)

[Verus](#)

[GUMBOX](#)

case REQ\_MHS\_3

[GUMBO](#)

[Verus](#)

[GUMBOX](#)

case REQ\_MHS\_4

[GUMBO](#)

[Verus](#)

[GUMBOX](#)

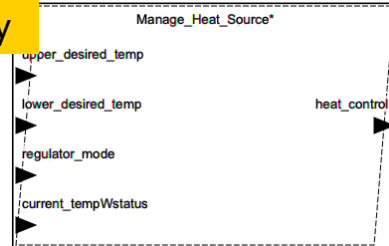
case REQ\_MHS\_5

[GUMBO](#)

[Verus](#)

[GUMBOX](#)

Req ID



## (Model) GUMBO contract clause for the requirement

```
Code Blame 623 lines (535 loc) · 31.7 KB
549
548 case REQ_MHS_1 "If the Regulator Mode is INIT, the Heat Control shall be
547 [set to OFF.
546 [http://pub.santoslab.org/high-assurance/module-requirements/reading/FAA-DoT-Requirements-AR-08-32.pdf#page=110 *]
545 assume regulator_mode == Isolette_Data_Model::Regulator_Mode::Init_Regulator_Mode;
544 guarantee heat_control == Isolette_Data_Model::On_Off::Off;
543
542
541
540 case REQ_MHS_2 "If the Regulator Mode is NORMAL and the Current Temperature is less than
539 [the Lower Desired Temperature, the Heat Control shall be set to On.
538 [http://pub.santoslab.org/high-assurance/module-requirements/reading/FAA-DoT-Requirements-AR-08-32.pdf#page=110 *]
537 assume (regulator_mode == Isolette_Data_Model::Regulator_Mode::Normal_Regulator_Mode)
536 & (current_temperature.degrees < lower_desired_temp.degrees);
535 guarantee heat_control == Isolette_Data_Model::On_Off::On;
534
533
532
531 case REQ_MHS_3 "If the Regulator Mode is NORMAL and the Current Temperature is greater than
530 [the Upper Desired Temperature, the Heat Control shall be set to Off.
529 [http://pub.santoslab.org/high-assurance/module-requirements/reading/FAA-DoT-Requirements-AR-08-32.pdf#page=110 *]
528 assume (regulator_mode == Isolette_Data_Model::Regulator_Mode::Normal_Regulator_Mode)
527 & (current_temperature.degrees > upper_desired_temp.degrees);
526 guarantee heat_control == Isolette_Data_Model::On_Off::Off;
525
524
523
522
```

## (Code - Verification) Rust/Verus contract clause for the requirement

```
78 // If the Regulator Mode is INIT, the Heat Control shall be
79 // [set to OFF.
80 // [http://pub.santoslab.org/high-assurance/module-requirements/reading/FAA-DoT-Requirements-AR-08-32.pdf#page=110 *]
81 (old(api).regulator_mode == Isolette_Data_Model::Regulator_Mode::Init_Regulator_Mode) ==>
82 (api.heat_control == Isolette_Data_Model::On_Off::Off);
83
84
85
86
87
88
89
90
91
92 case REQ_MHS_2
93 // If the Regulator Mode is NORMAL and the Current Temperature is less than
94 // [the Lower Desired Temperature, the Heat Control shall be set to On.
95 // [http://pub.santoslab.org/high-assurance/module-requirements/reading/FAA-DoT-Requirements-AR-08-32.pdf#page=110 *]
96 (old(api).regulator_mode == Isolette_Data_Model::Regulator_Mode::Normal_Regulator_Mode) &&
97 (old(api).regulator_status == Isolette_Data_Model::Status::On_Status) ==>
98 (api.heat_control == Isolette_Data_Model::On_Off::On);
99
100
101
102
```

## (Code Test) Executable contract clause in testing oracle for the requirement.

```
Code Blame 332 lines (307 loc) · 13.5 KB
129
130 /** guarantee REQ_MRI_2
131 * If the Regulator Mode is NORMAL,
132 * the Regulator Status shall be set to On
133 * http://pub.santoslab.org/high-assurance/module-requirements/reading/FAA-DoT-Requirements-AR-08-32.pdf#page=110 *]
134 * @param api_regulator_mode incoming data port
135 * @param api_regulator_status outgoing data port
136 */
137
138 pub fn compute_case_REQ_MRI_2(
139 api_regulator_mode: Isolette_Data_Model::Regulator_Mode,
140 api_regulator_status: Isolette_Data_Model::Status) -> bool
141 {
142 implies{
143 api_regulator_mode == Isolette_Data_Model::Regulator_Mode::Normal_Regulator_Mode,
144 api_regulator_status == Isolette_Data_Model::Status::On_Status
145 }
146 }
```

# Conclusions -- Themes

- Raising the abstraction level
  - “**patterns** for Microkit protection domains” **for application components**
  - choosing patterns to be amenable to component/system assurance
  - representing patterns/abstractions in **standardized modeling languages**
  - separating developer view of the pattern (higher-level) from seL4/microkit realization (lower-level)
- Auto-generation support for development tasks
  - build scripts, VM configuration, testing, logging
- Leveraging specifications for both verification and testing
- Integrating activities from broader industry ecosystems, especially those related to assurance activities

# Plans - Next Six Months

- System Reasoning
  - Formal system specifications
  - System Testing / Run-time Monitoring
  - System Verification
- Continued evolution of Microkit target
  - More systematic scheduling and communication, support for LionsOS concepts
- Efficiency improvements for seL4 microkit and hardening of infrastructure code
- Build-out for assurance framework, traceability, attestation